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Energy Transport Simulation with Quasi Three-Dimensional Temperature Analysis for SOI-MOSFET

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A new device simulator with energy transport analysis and quasi three-dimensional temperature analysis has been developed for evaluating the temperature rise in short channel SOI-MOSFET. A self-heating becomes a serious problem in short channel SOI-MOSFET owing to a small thermal conductivity of the buried oxide layer when the channel current is increased. We could accurately simulate various effects caused by the temperature rise such as the negative output resistance behaviour, the influence of the design rule on the temperature rise and the increase of the breakdown voltage due to the increased device temperature.

1. Introduction

SOI-MOSFET has been intensively investigated for achieving the sub-quarter micrometer or further scaled-down devices because it has a larger transconductance and shows the less short channel effect. However, self-heating is a serious problem in short channel SOI-MOSFET owing to a small thermal conductivity of the buried oxide layer when the channel current is increased. The temperature rise in the channel region by self-heating reduces the drain current in the saturation region and increases the drain breakdown voltage which is caused by the parasitic bipolar action. In order to precisely evaluate such temperature rise effect in short channel SOI-MOSFET, we developed a new device simulator with energy transport analysis and quasi three dimensional (3D) temperature analysis. In this simulator, the cylindrical coordinates are employed for solving the 3D heat flow equations with a fast computational turn-around time, because it is a very time-consuming calculation to solve the complete 3D heat flow equations in the wide region by the conventional method.

It is demonstrated in this paper that the newly developed device simulator for SOI MOSFET can describe the experimental results very well.

2. Simulation Algorithm

The simulation flow chart is shown in Fig. 1. In this flow chart, at the first, the device parameters such as the potential, carrier density, current, electron temperature and so on are calculated using 2D energy transport analysis[1]-[4]. Then, the power dissipation is calculated based on these results. This dissipation power is used when the heat flow equations are solved to obtain the temperature rise in the channel region. In this case,

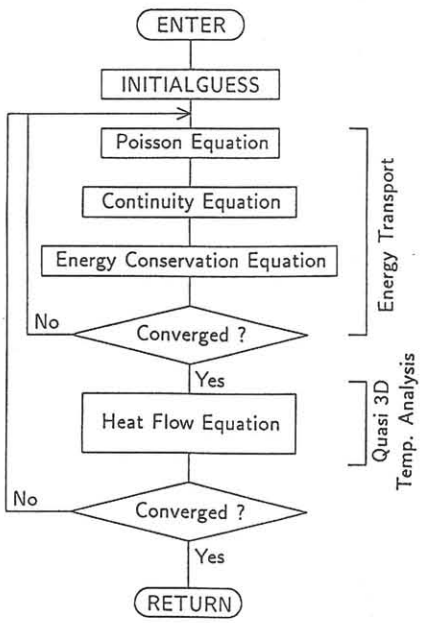

Fig. 1 Simulation flow chart.

the heat flow equation should be solved in the wide region and in 3D directions because the heat is diffused radially to a relatively long distance. However, it consumes a very long computational time to solve the complete 3D heat flow equations in the wide region. Then, we employ a new quasi 3D temperature analysis where the cylindrical coordinates are adopted for describing the radial heat flow and reducing the computational turn-around time as shown in Fig. 2. The doughnut meshes are used in the SOI, oxide and substrate silicon regions while the sector meshes are employed in the electrode regions. The device region is approximated by one small disk mesh which is placed in the center of the cylindrical coordinates. The dissipation power previously obtained is put into this small disk

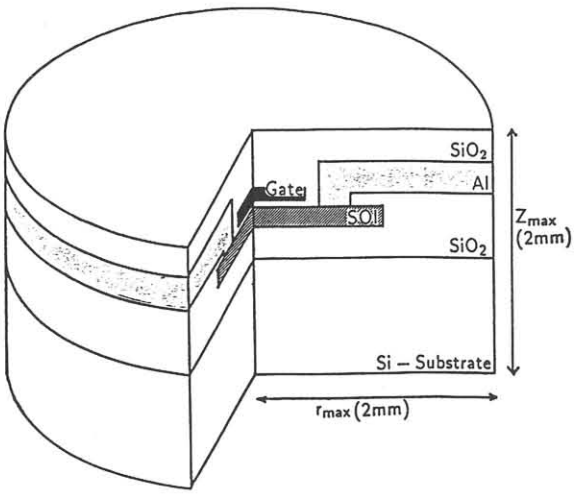

Fig. 2 Cylindrical coordinate for solving heat flow equations.

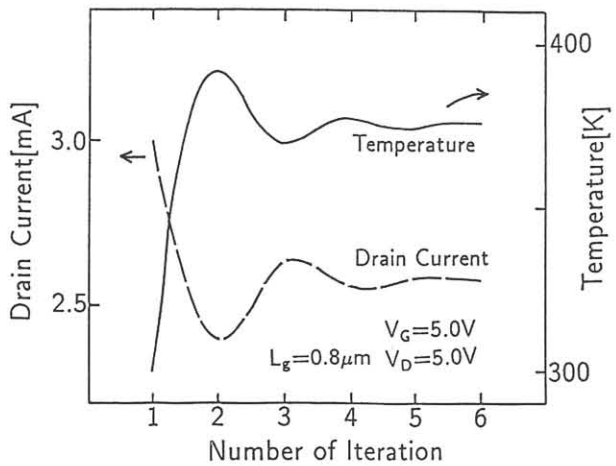

Fig. 3 Convergence of drain current and device temperature.

mesh when the heat flow equations are solved to obtain the device temperature. This temperature obtained is again used for solving device equations according to the energy transport analysis. Thus, we can obtain the device temperature in the steady state by repeating this procedure. Figure 3 shows the convergence of the solution with the number of iteration in the calculation of the drain current and the device temperature. As is clear in the figure, the final solution is easily obtained after five or six iterations.

3. Results and Discussions

The I_D-V_D characteristics of n-channel LDD SOI-MOSFET with the gate length of 0.8μm are shown in Fig. 4 where the simulation results with and without the quasi 3D temperature analysis are compared with the experimental ones. The simulation results with the quasi 3D temperature analysis indicate the excellent agreements with the experimental ones. It is noted that the negative output resistance behaviors in the higher gate voltage region are expressed very well by the simulation with the quasi 3D temperature analysis while the simulation without the temperature analysis shows no negative output resistance. The device tempera-

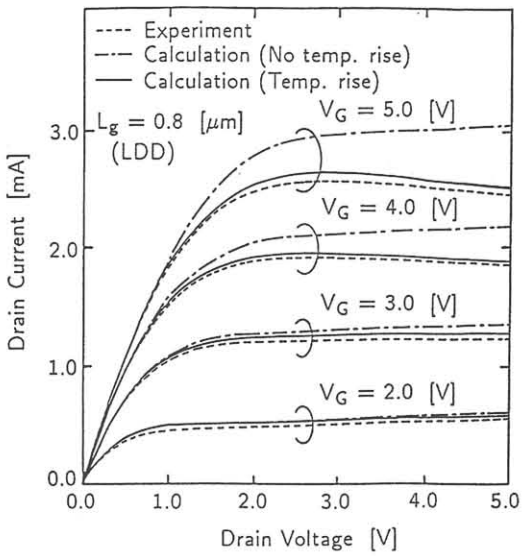

Fig. 4 Drain current-voltage characteristics in n-channel LDD SOI MOSFET.

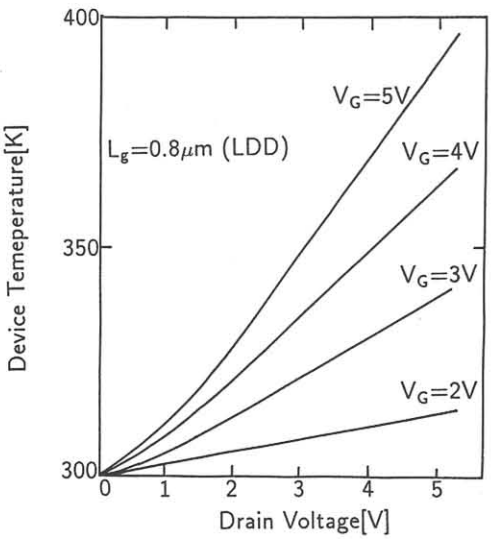

Fig. 5 Device temperature vs. drain voltage relation in n-channel LDD SOI MOSFET.

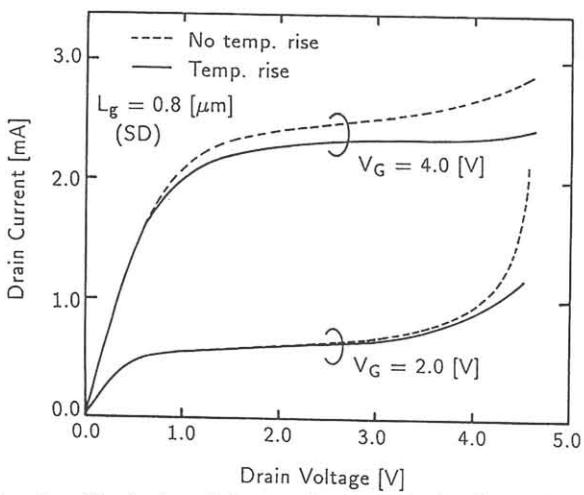

Fig. 6 Drain breakdown characteristics in n-channel single drain SOI MOSFET.

ture is plotted as a function of the drain voltage in Fig. 5. As is obvious from the figure, the de-

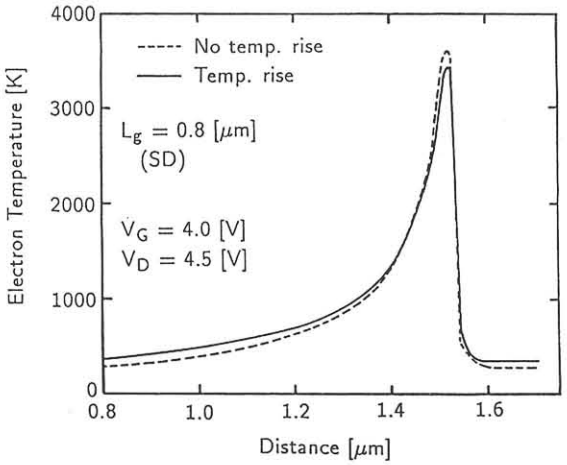

Fig. 7 Electron temperature distribution along the channel of n-channel single drain SOI MOSFET.

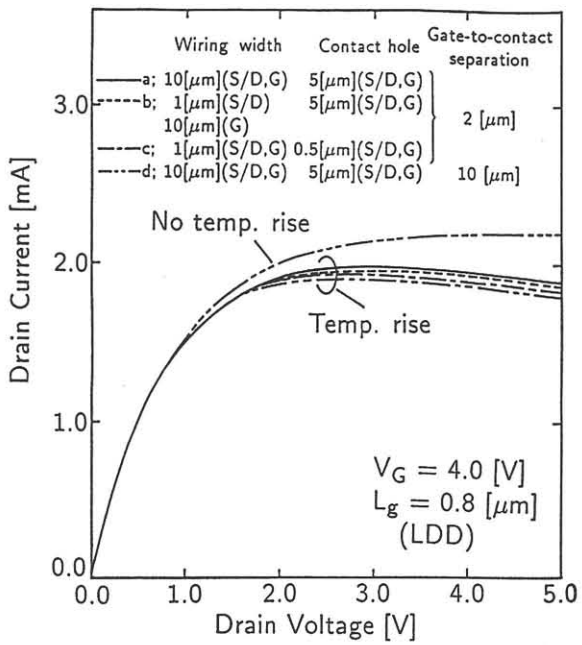

Fig. 8 The influence of the design rule and the device layout on I_D-V_D characteristics.

vice temperature significantly rises with increasing V_D and V_G. We can also simulate the increase of the drain breakdown voltage, which results from the increased device temperature, by using our new device simulator as shown in Fig. 6. The maximum electron temperature at the drain junction edge near the gate is reduced by the increase of the device temperature as shown in Fig. 7. Consequently, the impact ionization probability is reduced and the drain breakdown voltage is increased. The device temperature is influenced by the design rule and the device layout. Figure 8 shows how the device temperature is influenced by the Al wiring width, the contact hole size and the gate-to-contact hole separation. It is clearly simulated that the device temperature rise is more significant as the wiring width is narrower, the contact hole size is smaller, and the gate-to-contact hole separation is longer. The influences by the adjacent devices can be also simulated using our new device simulator. The device temperature rise by the adjacent devices

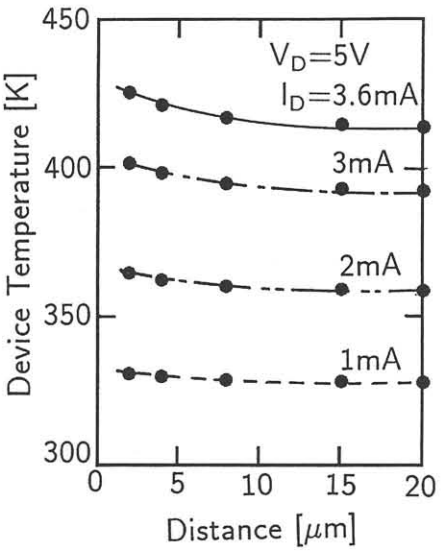

Fig. 9 Device temperature vs. distance between the devices.

is plotted as a function of the distance between the devices in Fig. 9 where it is assumed that one device is surrounded by four devices apart from a equal distance. The temperature of the device in the center is plotted in the figure. All five devices are operated at the same condition in this example. It is clear in the figure that the device temperature is increased around several kelvin to a few ten kelvin by the adjacent devices. However, the influences by the adjacent devices are eliminated when the distance between the devices is increased to more than 20μm.

4. Conclusion

We developed a new device simulator with energy transport analysis and quasi 3D temperature analysis for evaluating the temperature rise due to self-heating in SOI-MOSFET. We could accurately simulate the negative output resistance behavior, the increase of the breakdown voltage due to the increased device temperature and the influence of the design rule on the temperature rise with a fast computational turn-around time.

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