Phosphorus-Implanted Polysilicon Emitters with High Emitter Efficiency

A. Pruijmboom, W.T.A. van den Einden, D.B.M. Klaassen, J.W. Slotboom, G. Streutker, A.E.M. de Veirman, P.C. Zalm

> Philips Research Laboratories, P.O.Box 80.000 5600JA Eindhoven, The Netherlands

Phosphorus-doped polysilicon emitters have been fabricated with a low emitter series resistance and an emitter efficiency that is 4-5 times higher than that of arsenic-doped polysilicon emitters. These emitters have been realized using conventional ion implantation and rapid thermal annealing. We present a model, which explains the magnitude as well as the temperature dependence of the hole-recombination current in these emitters. This model predicts, in agreement with our experiments, that the emitter efficiency increases for shallower emitters. We also elucidate the difference between arsenic and phosphorus-doped polysilicon emitters.

Introduction

Recently, Kondo et al. [1] and Nanba et al. [2] have shown that, with in-situ phosphorus-doped amorphous silicon, very shallow emitters can be made with a very high emitter efficiency and a low emitter series resistance. Here, we show that a similar result can be achieved, using standard polysilicon deposition, phosphorus implantation and RTA annealing. We present a model, which explains the magnitude, as well as the temperature dependence, of the hole-recombination current in these emitters. Furthermore, we show that the difference between arsenic and phosphorus-doped polysilicon emitters can be explained in terms of perforation of the interfacial barrier between mono- and polysilicon.

Experiments and Results

In a non-selfaligned transistor structure, the base was introduced by a 10 keV B implantation in monosilicon, with doses of 1.2, 2.4 and 3.6×10^{13} cm⁻², and annealed for 20 minutes at 900 °C. For emitter formation, a 200 nm-thick CVD polysilicon layer was deposited after HF dipping and implanted with P, using a dose of 1.0×10^{16} cm⁻². RTA annealing, at temperatures between 900 and 975 °C, during 7 seconds, was used for emitter outdiffusion into the monosilicon. As a reference, one of the wafers was not implanted with P but with 1.0×10^{16} cm⁻² As. This wafer was RTA annealed 7 seconds at 1100 °C.

Figure 1 shows very shallow P profiles obtained by SIMS, displaying junction depths of 58 nm and



Figure 1: SIMS of P and B, from emitter area, annealed at 900 (solid line) and 975 °C (dashed line).

70 nm for transistors annealed at 900 and 975 °C, respectively. The effective emitter Gummel number G_E of our transistors, shown in fig. 2, ranges between 54 and $82 \times 10^{12} \text{ s} \cdot \text{cm}^{-4}$. G_E increases for decreasing annealing temperature and for increasing base doping. Both trends correspond to a higher G_E for a shallower emitter-base junction. G_E of the As-doped emitter is $18 \times 10^{12} \text{ s} \cdot \text{cm}^{-4}$. The 4-5 times higher G_E for the Pdoped emitters is also reflected in the Gummel plot of fig. 3, which shows ideal base-current characteristics. The emitter resistance R_E did not show a dependence on the annealing temperature. $R_E = 33(\pm 5)\Omega\mu^2$, for both the P and As-doped emitters, as obtained from measurements on transistors with emitter areas



Figure 2: Emitter Gummel number vs. annealing temperatures of P-doped polysilicon emitter. Circles, squares and triangles correspond to baseimplantation doses of 1.2, 2.4 and 3.6×10^{13} cm⁻², respectively. Error bars denote variations over the wafers.

of 4 and 120 μ m².

The high G_E - combined with low R_E -values indicate the presence of a very effective hole barrier at the poly-mono interface, that does not act simultaneously as an electron barrier. The effective surface recombination velocity S_{eff} at the poly-mono interface was determined from a comparison of measured base currents with 1D-device simulations, using the doping profile obtained by SIMS [3] (see fig 4). For the As-doped emitters S_{eff} is quite high and only weakly dependent on temperature. For the P-doped emitters, however, S_{eff} shows a strong dependence on temperature and is much lower. These low values



Figure 3: Gummel plot of transistors with As (solid line) and P-doped (dashed line) polysilicon emitter.



Figure 4: S_{eff} of As (dots) and P-doped (circles) polyemitter. Solid line: eq. 1, dashed line: $S_{eff} = v_{tr}$.

of S_{eff} indicate that, even for these very shallow emitters, recombination in the monosilicon is the main origin of the base current. This explains why the shallower P-doped emitters have the higher G_E .

Interpretation and Discussion

Assuming that the hole-diffusion length in the polysilicon is much smaller than the poly thickness, S_{eff} is given by

$$S_{eff} = \frac{v_d v_{tr}}{v_d + v_{tr}} \tag{1}$$

Here, v_d is the minority diffusion velocity in the polysilicon and v_{tr} is the velocity at which holes cross the interface from mono to poly and from poly to mono. For the P-doped emitter S_{eff} exhibits over more than one decade an exponential dependence on the inverse temperature. This suggests that thermionic emission of holes with mass m over a potential barrier with height Φ_B is the predominant transport mechanism and, hence,

$$v_{tr} = \sqrt{\frac{kT}{2\pi m}} \exp(-\frac{q\Phi_B}{kT}) = v_{tr,o} \exp(-\frac{q\Phi_B}{kT}) \quad (2)$$

Fitting eqs. 1,2 to the values of S_{eff} (solid lines in fig. 4) yields for the P-doped emitter : $\Phi_B=220 \text{ mV}$, $v_d = 4 \times 10^5 \text{ cm} \cdot \text{s}^{-1}$ and $v_{tr,o} = 3 \times 10^7 \text{ cm} \cdot \text{s}^{-1}$, while for the As-doped emitter $\Phi_B = 75 \text{ mV}$, $v_d = 2 \times 10^6 \text{ cm} \cdot \text{s}^{-1}$ and $v_{tr,o} = 3 \times 10^6 \text{ cm} \cdot \text{s}^{-1}$ is found. The values of $v_{tr,o}$ and v_d found for the P-doped emitter are reasonable, but especially the large difference in the values of $v_{tr,o}$ found for P and As-doped emitters (extrapolation of dashed lines to $T^{-1} = 0$) seems unphysical. Inspection of the poly-mono interface of both emitters (see HRTEM fig. 5) points, however, to



Figure 5: HRTEM of poly-mono interface of As (a) and P-doped (b) polyemitter.

a plausible explanation: for the P-doped emitter a continuous amorphous layer is visible between the poly- and monosilicon, while for the As-doped emitter the interface has been reconstructed and, on the recrystalized areas, gaps are visible in the amorphous layer.

To investigate the effects of such γ_{conf} for a developed an analytical method to calculate S_{eff} for a 2D homogeneously doped emitter. This rather simple method allows extensive variations of parameters and reproduces the results of 2D device simulations [4, 5]. In fig. 6 the results are shown found for S_{eff} of a 1 μ m-wide emitter, as a function of the



Figure 6: Dashed lines: calculated S_{eff} as a function of the transparency (Tr) and number of gaps (#). Solid line: eq. 1.

transparency (i.e. fraction of the surface where no barrier exists) and the number of gaps. In this calculation the transport across the barrier from the poly to the mono was neglected, leading to a S_{eff} not limited by v_d at high T. This procedure is justified by the observation that for a perforated barrier diffusion through the gaps is the dominant transport mechanism and the details of the intact interfacial regions are of secondary importance [4]. From fig. 6 we see that a relatively low transparency divided over only a few gaps, is indeed sufficient to explain the difference between the P and As-doped emitters.

Conclusions

In our phosphorus-implanted polysilicon emitters a hole barrier at the poly-mono interface suppresses hole injection into the polysilicon. This results in a hole current which, at room temperature, is dominated by recombination in monosilicon. Consequently the shallower phosphorus-doped emitters have higher effective emitter Gummel numbers.

The higher value and the weaker temperature dependence of the base current in our arsenic-doped emitters is explained by perforation of the interfacial barrier.

Acknowledgement

This research was partly supported by ESPRIT project 2016 "TIPBASE".

References

- M. Kondo et al., 1991 Symposium on VLSI technology, Digest of Technical Papers, pp. 65-66, 1991.
- [2] M. Nanba, et al., IEDM 91 Techn. Dig., pp. 443-446, 1991.
- [3] G. Streutker et al., to be presented at BCTM'92.
- [4] J.L. Egley and J.L. Gray, IEEE Trans. Electron Dev. 38 (1991), 2112.
- [5] J.S. Hamel et al., IEEE Electron Dev. Lett. 13 (1992), 114.