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Temperature Dependence of the DC and High Frequency Properties of HEMTs with Sub 0.1 μm Gatelength

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We report on the fabrication and temperature dependent electrical characterization of HEMTs with gatelengths L_G down to 45 nm. The HEMTs were fabricated on modulation doped pseudomorphic ($GaAs/In_{0.2}Ga_{0.8}As$) and lattice-matched ($In_{0.53}Al_{0.47}As/In_{0.53}Ga_{0.47}As$) heterostructures. The high frequency properties of these devices were measured from room temperature to T=100 K using on-wafer-probes in a setup specialized for low temperature operation. The electrical characteristics of the samples and the HEMTs exhibit a strong temperature dependence, which can be used as an additional information to reveal the length scale dependent electron transport properties of the heterostructures.

High speed field effect transistors operating at microwave frequencies are attractive devices for physical investigations and for various application purposes. Si-based MOSFETs have achieved very good performance [1, 2] but III-V heterostructure HEMTs yield even higher transition frequencies and lower noise figures [3, 4, 5].The charge carrier transport in ultra-short gate length FETs may be enhanced by velocity overshoot and is therefore of special physical interest. Temperature dependent high frequency characterization [6, 7, 8] of HEMTs gives valuable information about the carrier transport beneath the gate and does not rely on a complex numerical process, as Monte Carlo simulations do.

Pattern definition for the HEMT fabrication process was accomplished using electron beam lithography for all layers. Beam currents were varied from 5 nA for coarse patterns to 200 pA for the fine gate structures; beam acceleration voltage was 50 kV. The lithography of our process involves exposures of e-beam alignment marks, mesas for device isolation, ohmic contact regions, macroscopic contact pads and the gates. For mesa definition an elctron-beam and postbake induced image reversal process of the positive tone AZ 5214 photoresist was used. For the T-gate fabrication we applied a double layer resist consisting of PMMA and its copolymer P(MMA-MAA). A SEM photograph of a gate with 45 nm gatelength is shown in Fig. 1.

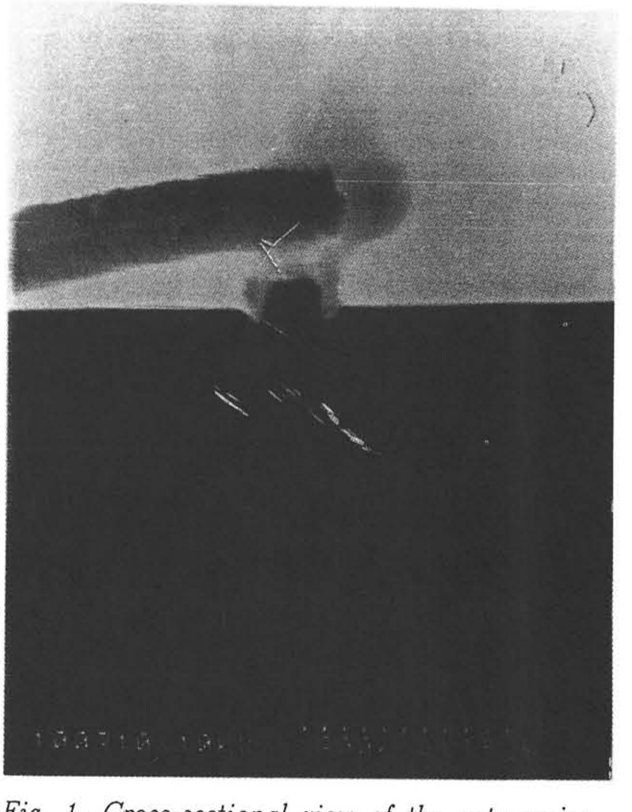

Fig. 1. Cross-sectional view of the gate region. Gatelength is 45 nm; the top of the 'T' was torn off by cleaving the sample.

To characterize the HEMTs at low temperatures in the HF regime we measured the scattering parameters with a vector network analyzer (VNA) and on-wafer probeheads. For control of the measurement temperature, we used a liquid Nitrogen cooled wafer chuck operating in a dried gas atmosphere. A sketch of the setup is given in Fig. 2. The top of the chuck, the wafer probes and the microscope objective were wrapped with a plastic foil, thus forming a closed volume.

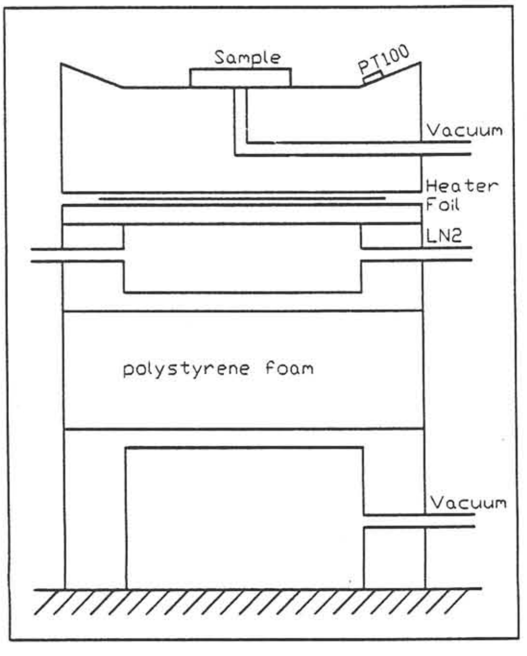

Fig. 2. Cross-section of the waferchuck for low-temperature DC and high frequency measurements.

This volume was purged with a dried and heated ($\approx$ 330 K) Nitrogen gas flow. The gas flow eliminates any moisture and ensures an environmental temperature for the probeheads of $\approx$ 300 K, while the temperature of the wafer chuck surface can be reduced to 100 K. The accuracy of the room temperature calibration of the VNA was verified by s-parameter measurements of an offset short at T=300 K and T=100 K. As shown in Fig. 3, the ratio of the 300 K and 100 K data demonstrates that the measurements agree very well within a maximum deviation of 3%. This allows for precise temperature dependent on-wafer s-parameter measurements.

The best obtained extrinsic 300 K (100 K) values of g_m and f_t amount to 720 mS/mm (1130 mS/mm) and 145 GHz (240 GHz), respectively. To remove fabrication-technology related effects, we measured the source resistances and computed the intrinsic transconductance $g_{m,i}$. As can

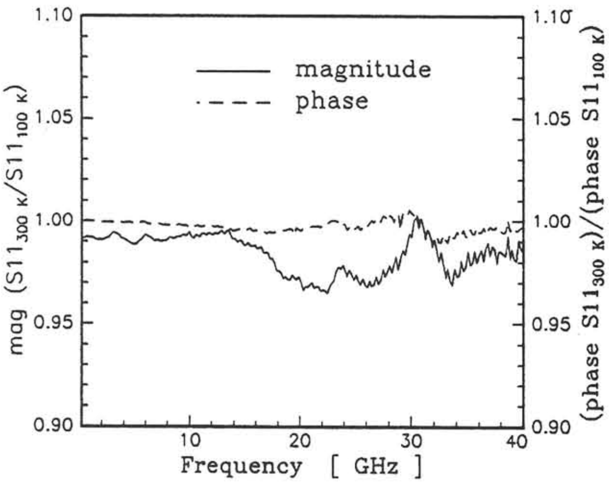

Fig. 3. Ratio of two s-parameter measurements of an offset short at T=300K and T=100K. The left axis gives the amplitude ratio, the right one the phase ratio.

be seen from Fig. 4, the $g_{m,i}$ values reflect directly the decrease of electron scattering mechanisms with decreasing temperature; furthermore, the superior transport properties of the lattice-matched heterostructure are demonstrated for the whole temperature range.

We determined the electron propagation velocity v_e by calculating the intrinsic transition frequency $f_{t,i}$ and using the short channel approximation $v_e=2\cdot\pi\cdot f_{t,i}\cdot L_G$. To get accurate values for $f_{t,i}$, we fitted the measured s-parameters to an equivalent circuit which includes pad capacitances. An important result of this analysis is that the source-to-gate capacitance is proportional to L_G with an offset in the range of 30 nm to 60 nm which depends on material and recess depth. The temperature profiles of v_e, extracted from a HEMT with 45 nm gatelength, and the saturation velocity $v_{e,s}$ extracted from a macroscopic Hall structure is given in Fig. 5. The value of v_e raises more rapidly than that of $v_{e,s}$; the temperature dependence of both velocities can be fitted according to $v_{e(,s)} \sim T^p$ with p_e=-0.65 for v_e and $p_{e,s}$=-0.52 for $v_{e,s}$. On the other hand, for gate lengths of 55 nm and above, p_e equals to the value of $p_{e,s}$. This indicates that electron transport in our HEMTs is mainly determined by saturation velocity for these gatelengths. For the shortest gates and at low temperatures, deviations from saturated carrier velocity occur, indicating the onset of velocity overshoot.

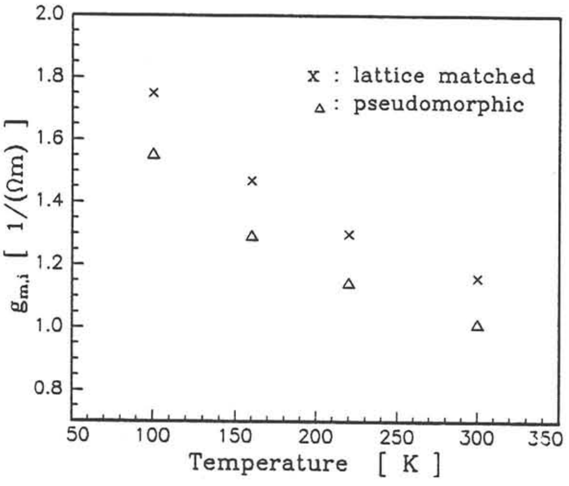

Fig. 4. Temperature dependence of the intrinsic transconductance of HEMTs with L_G=*45 nm on pseudomorphic and lattice matched heterostructures.*

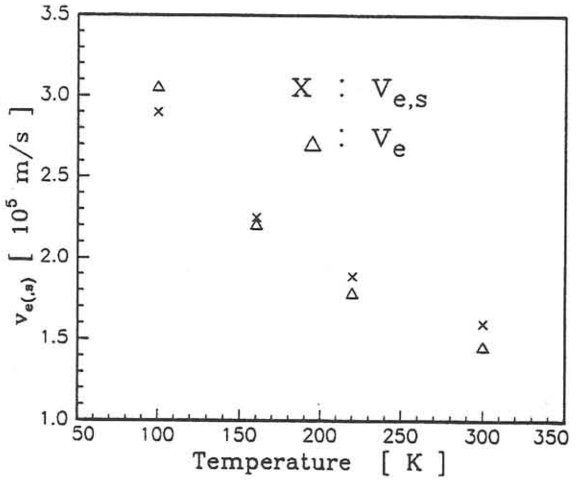

Fig. 5. Temperature dependence of the electron saturation velocity $v_{e,s}$ *obtained from Hall measurements and of* v_e *obtained from a HEMT with 45 nm gate length on the lattice matched heterostructure.*

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