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High-Performance InAlAs/InGaAs HEMTs and Their Application to a 40-GHz Monolithic Amplifier

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We have achieved state-of-the-art low-noise performance by applying ultra-low-noise 0.15-μm-gate InAlAs/InGaAs HEMTs on InP passivated with silicon nitride to a 40-GHz monolithic amplifier. A HEMT has shown a minimum noise figure of 0.55 dB at 26 GHz with an associated gain of 9.2 dB. The monolithic two-stage amplifier achieves a noise figure of 2.7 dB at 40 GHz with a gain of 10.6 dB. The noise figures range 2.4 - 2.8 dB with a gain of 10.6 - 11.6 dB from 34 to 40 GHz.

1. Introduction

Due to the excellent carrier transport properties of the $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ heterostructure, InAlAs/InGaAs HEMTs lattice matched to InP have excellent high-frequency and low-noise performance. For example, U. K. Mishra et al. reported an f_T of 250 GHz with a 0.12-μm-gate-length HEMT[1]; K. H. G. Duh et al. reported a minimum noise figure of 0.8 dB at 60 GHz with a 0.1-μm-gate-length HEMT[2]; and P. C. Chao et al. reported 0.3 dB at 18 GHz with a 0.15-μm-gate-length HEMT[3]. Over the past few years we have been studying InAlAs/InGaAs HEMTs and have achieved a f_T of 200 GHz with a 0.12-μm-gate-length HEMT[4,5] and a minimum noise figure of 0.43 dB at 26 GHz with a 0.18-μm-gate-length HEMT[6]. We have also reported that these performances can be explained by the saturation velocity of 2.7×10^7 cm/s [7]. As for the application to monolithic-microwave-integrated-circuit (MMIC) low-noise amplifiers, P. K. Smith et al. reported a noise figure of 3.0 dB at 63 GHz for a monolithic two-stage amplifier with 0.15-μm-gate-length HEMTs[8]; and E. Soverto et al. reported a noise figure of 7.0 dB for a monolithic three-stage amplifier that also used 0.15-μm-gate-length HEMTs[9]. However, the former amplifier is incomplete as a monolithic amplifier because it does not contain input matching circuit, and the latter one does not make the most of potential ultra-low-noise characteristics of InAlAs/InGaAs HEMTs.

In this paper, we report a monolithic low-noise amplifier that achieves state-of-the-art low-noise performance with InAlAs/InGaAs HEMTs. It includes all the elements necessary for MMICs such as input/output matching and biasing circuits. Besides the HEMTs, low-loss coplanar waveguides also contribute to the low-noise performance of the amplifier.

2. InAlAs/InGaAs HEMT

The InAlAs/InGaAs heterostructure[4,5] was grown by MBE and exhibited a high mobility of 10,000 $cm^2V^{-1}s^{-1}$. To reduce gate resistance and improve the RF and noise performance of the HEMT, the footprint of the T-shaped gate was delineated by single-resist electron-beam lithography and the large top portion was delineated by optical lithography. Using this fabrication process, a very fine footprint and very large top portion of the 0.15-μm-long T-shaped gate (Fig. 1) were formed and resulted in DC gate resistance as low as 85 Ω/mm end to end. A multifinger gate pattern using gate-source air bridges was used to reduce gate resistance further. A silicon nitride film

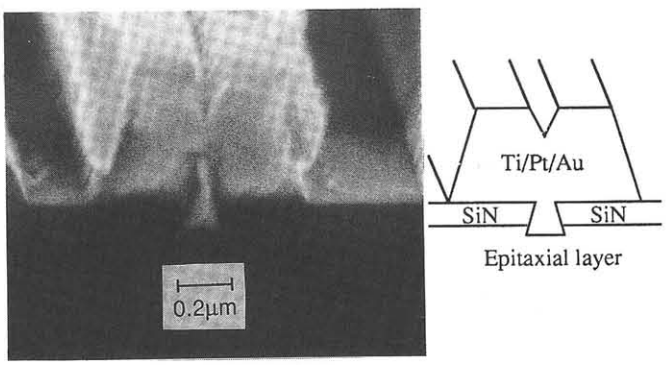

Fig. 1 SEM micrograph of 0.15-μm-length T-shaped gate.

was deposited on the surface of the epitaxial layer to protect the heterostructure during fabrication and to support the large top portion of the T-gate. The use of a novel n^+-InGaAs/n^+-InAlAs cap layer[5,6] to reduce the ohmic contact resistance of the non-alloyed ohmic contact resulted in a low ohmic contact resistance of 0.06 Ω•mm, a low sheet resistance for all layers of 160 Ω/sq, and a low source resistance of 0.14 Ω•mm. Figure 2 shows I-V characteristics of a 0.15 x 50-μm^2-gate device revealing

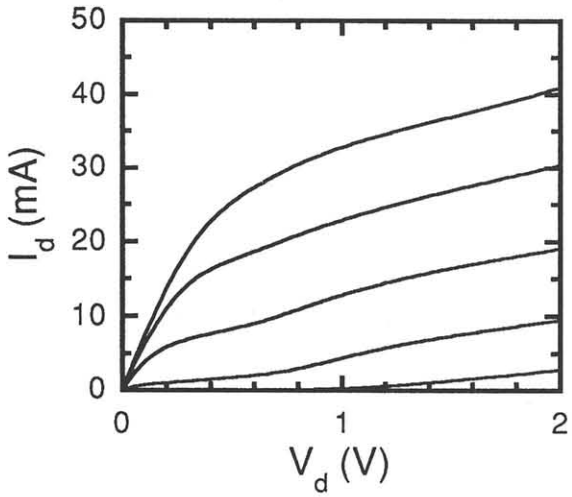

Fig. 2 DC I-V characteristics of 0.15 x 50 μm^2 HEMT. Gate voltage ranges from -0.8 to 0 V in 0.2-V increments.

transconductance, g_m, as high as 1000 mS/mm at a drain bias of around 1 V. For a 100-μm-wide 8-gate-finger device, the cutoff frequency, f_T, was 126 GHz, the maximum oscillation frequency, f_{max}, was 220 GHz at a drain voltage, V_d, and current, I_d, of 1.1 V, 55 mA, respectively. This f_T is lower than the 160 GHz with a 0.15-μm-gate-length HEMT we reported previously[4]. The decrease in f_T can be explained by the increase in parasitic capacitance with the passivation, which is 170 fF/mm for gate-source and gate-drain, respectively[6]. The minimum noise figure, F_{min}, was as low as 0.55 dB at 26 GHz with an associated gain, G_{as}, of 9.2 dB at V_{ds} = 0.8 V, I_{ds} = 15 mA. The HEMT showed a high f_T and f_{max} of 91 GHz and 184 GHz, respectively, even at a bias of F_{min}.

3. Low-noise Amplifier

Figures 3 and 4 show the schematic circuit diagram and photograph of the 40-GHz monolithic two-stage low-noise amplifier. The chip is 1.4 x 0.88 mm^2 and consists of 50-μm-wide 4-gate-finger HEMTs, coplanar waveguides for I/O matching stubs at each stage, and biasing circuits including metal-insulator-metal (MIM) capacitors and resistors with active layers. The design of this amplifier circuit is based on the uniplanar circuit configuration[10] that enables circuits to be fabricated on one side of the substrate so that the fabrication process is simpler than the process used in conventional circuit configuration with microstrip lines and via holes. Circuit

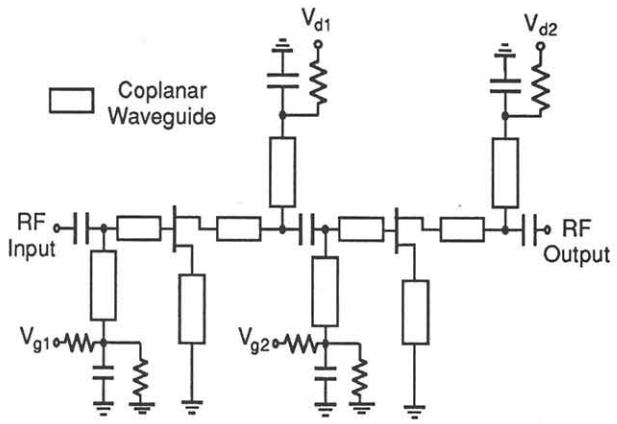

Fig. 3 Schematic diagram of two-stage amplifier.

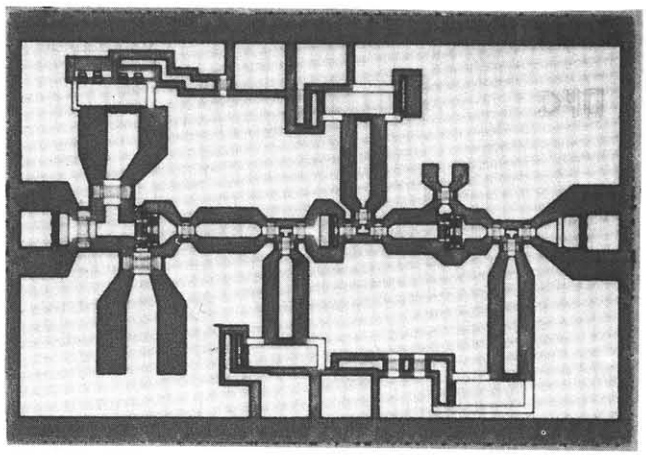

Fig. 4 Photomicrograph of two-stage amplifier. Chip size is 1.4 x 0.88 mm^2.

simulation revealed that waveguide loss at the input matching stubs affects the noise figure, NF, of the amplifier but that waveguide loss at inter-stage and output matching stubs hardly affects NF. Therefore, wide coplanar waveguides with an 80-μm center strip and 60-μm gap were designed for the input matching stubs to reduce waveguide loss, whereas waveguides for other stubs have a 40-μm center strip and 30-μm gap. The noise figure of an amplifier employing the wider coplanar waveguides was calculated to be about 0.1 dB lower than one employing the narrow ones. The NF and gain, G, are plotted against frequency in Fig. 5. The amplifier achieved as low as 2.7 dB NF at 40 GHz with G = 10.6 dB. It also showed a less than 2.8 dB of NF and G = 10.6 - 11.6 dB from 34 to 40 GHz and kept more than 10 dB gain up to 43 GHz. The lowest NF was 2.4 dB at 38 GHz with G = 10.7 dB. The VSWR for the input and the output of the amplifier are plotted against frequency in Fig. 6. Sufficiently low VSWR of 1.5 and 2.0 for the input and the output port, respectively, was attained between 34 and 40 GHz with the amplifier.

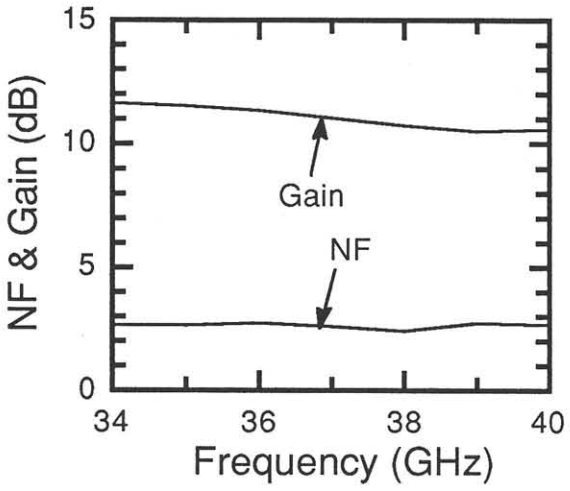

Fig. 5 Noise figure and gain of two-stage amplifier.

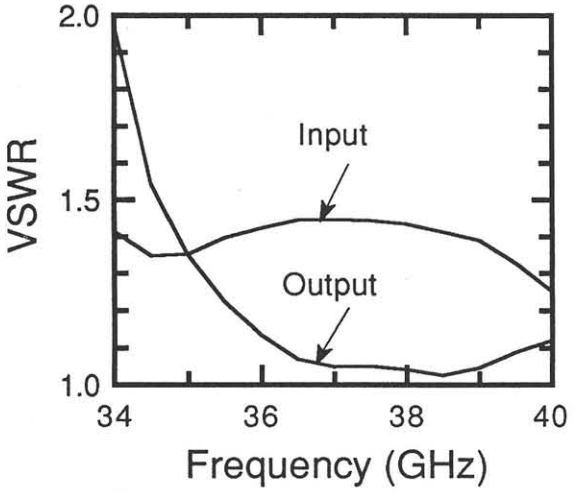

Fig. 6 VSWR for the input and output of two-stage amplifier.

4. Conclusion

0.15-μm-gate-length InAlAs/InGaAs HEMTs passivated with SiN have been fabricated and F_{min} = 0.55 dB with G_{as} = 9.2 dB has been achieved with a 100-μm-wide 8-gate-finger device. This HEMT has been applied to a monolithic two-stage low-noise amplifier which showed a NF = 2.7 dB with G = 10.6 dB at 40 GHz. The amplifier also showed a less than 2.8 dB of NF and G = 10.6 - 11.6 dB from 34 to 40 GHz. The amplifier's lowest NF was 2.4 dB at 38 GHz with G = 10.7 dB. To our knowledge, this is the lowest noise figure ever reported for 40-GHz monolithic amplifiers. Circuit simulation has revealed that NF of an amplifier employing a wider coplanar waveguide with an 80-μm center strip and 60-μm gap for the input stubs is about 0.1 dB lower than NF with a 40-μm center strip and 30-μm gap.

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