Parallel Data Inspection Operation in Three-Dimensional Content Addressable Memory with Optical Interconnection

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Three-dimensional content addressable memory with optical interconnection (3D-OCAM) has been proposed for the new parallel processing computer system. The 3D-OCAM is used to control the data transfer among many memory layers of three-dimensional memory LSI in this system. The vertical and horizontal data inspection operations among many memory layers are simultaneously implemented in 3D-OCAM. The test chip of 3D-OCAM was fabricated and its basic parallel inspection operation was successfully demonstrated.

1. Introduction

A multiprocessor system is the most promising way to achieve the high overall speed in computation and to maintain the system reliability. Many CPUs are connected to the common bus through respective cache memories in the bus-connection type multiprocessor system. The cache memories which act as common memories are used to share the same data among many CPUs. However, in order to share the data, the data written into one cache memory are transferred and copied to other cache memories through the common bus. As a result, the performance of such bus-connection type multiprocessor system is limited by the data communication efficiency of the common bus. To overcome this problem, it is very useful to implement the parallel data transfer among many cache memories. Then, we propose to use the optical interconnection for such parallel data transfer and furthermore a new content addressable memory with the optical interconnection to control the parallel data transfer among many cache memories [1]-[4]. We can control the data transfer so as to partially share the data among the limited numbers of cache memories by using this new content addressable memory as well as the data can be completely shared among all cache memories. This new content addressable memory with optical interconnection is called an optically coupled three-dimensional content addressable memory (3D-OCAM) [5],[6].

In this paper, the parallel data inspection operation of 3D-OCAM for the new multiprocessor system is mainly discussed.

2. Multiprocessor System with 3D-OCAM

Figure 1 depicts an example of a parallel processing computer system with 3D-OCAM. This
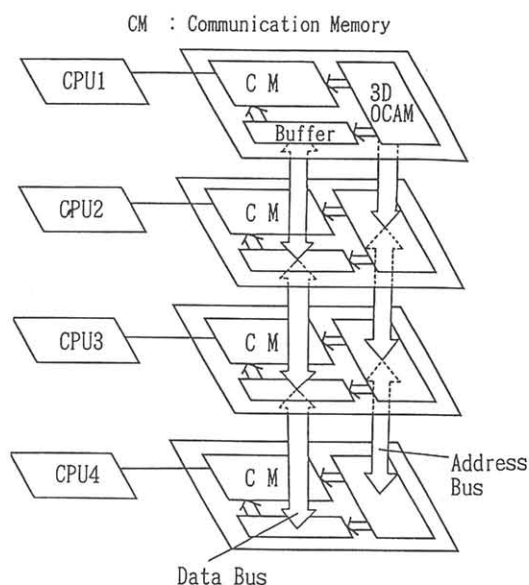

Fig. 1 Parallel Processing computer system with 3D-OCAM

system consists of many CPUs and three-dimensional memory LSI. The communication memory, buffer memory, and 3D-OCAM are integrated in each memory layer of 3D memory LSI. A memory layer is connected with the upper and lower memory layers by the optical interconnections in the buffer memories and the 3D-OCAM. The shared common data are transferred among the buffer memories through the optical interconnection in the vertical direction which acts as the data bus. The address tags are also transferred through the optical interconnection in the 3D-OCAM. In this case, the optical interconnection acts as the address bus. The address reference tables are installed in the 3D-OCAM. The communication memories which can be considered as cache memories are used to store the common

data. The address data for the communication memories are stored in the address reference tables. The memory layers where the common data are transferred are determined by the the address tags. The address tags are compared with the address data of the address reference tables in the respective memory layers of 3D-OCAM and the flags are generated when both data in the address tags and the address reference tables are matched. The data transfers from the buffer memories to the communication memories are commenced by these flags. Thus, the common data are written into the communication memories where sharing the data is required. A CPU is connected to the communication memory of the respective memory layer. Consequently, many CPUs can simultaneously execute different instructions sharing with the same data. Thus, the 3D-OCAM has a very important role to control the data transfer in the multiprocessor system shown in Fig.1.

3. Concept of 3D-OCAM

The optical data transfer in the 3D-OCAM and the buffer memory is carried out by using an optically coupling flip-flop (OC-FF) as shown in Fig.2. The OC-FF consists of the data store portion and the data transfer portion. The flip-flop with silicon photo diodes is used in the data store portion. Two LEDs are included in the data transfer portion. The data are optically transferred by this LED to the upper and lower memory layers. When the transferred light signal impinges onto either of two photo diodes in the upper or lower memory layer, the node voltage of the data store flip-flop is inverted. Thus, the transferred data are directly written into the data store flip-flop. The memory cell and peripheral circuits of 3D-OCAM are illustrated in Fig.3. The memory cell consists of three parts for data storage, data matching and data transfer. Each data in the address reference table is stored in the data storage part. The OC-FF is employed in the data transfer part. The address tags are transferred in the vertical direction by op-
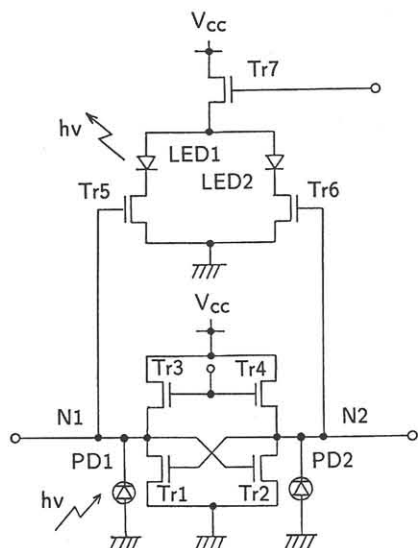

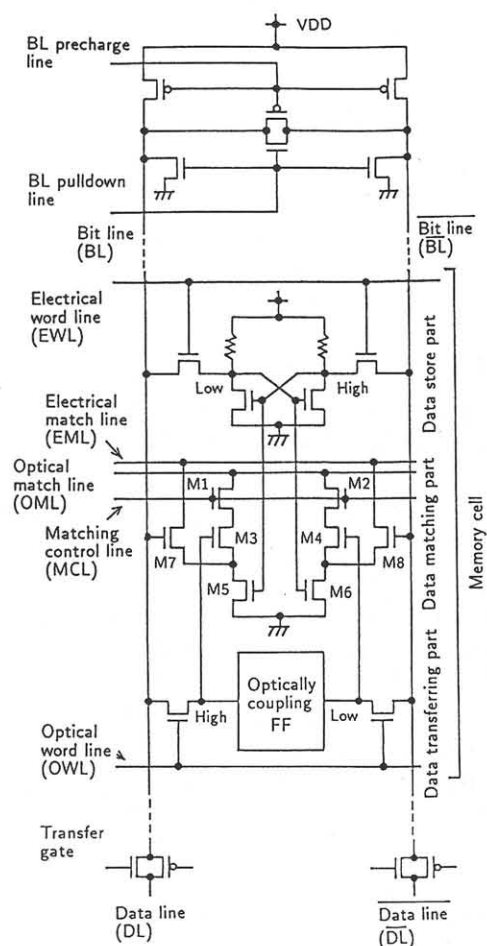Fig. 2 The optically coupling flip-flop for optical data transfer.

Fig. 3 Memory cell and peripheral circuits of 3D-OCAM.

tical coupling, storing them in the OC-FF. In the matching part, the address data in the data storage part is compared with the address tag stored in the data transfer part for the vertical inspection through all memory layers. The data in the data storage part can be also compared with those given to the bit lines for the horizontal inspection inside a memory layer. Both vertical and horizontal inspections are simultaneously implemented in parallel.

4. Fabrication of 3D-OCAM Test Chip

Two new technologies have to be developed to achieve 3D-OCAM. One is the technology to integrate LEDs on silicon LSI chip and the other is the 3D LSI technology. Monolithic approach using GaAs-on-Si technology or hybrid one can be employed to integrate LEDs. In this experiment, LEDs with 0.85um wave length are placed above the silicon test chips. As for the 3D LSI technology, we could stack six thinned device wafers with the alignment tolerance of 1um by using the newly developed 3D wafer aligner [7]. Each wafer was thinned to around 5um by using a mechano-chemical polishing technique where the polishing is automatically stopped by the oxidized trenches. The SEM cross section of such 3D test chip is shown in Fig.4. The SEM micrograph of 3D-OCAM test circuit is shown in Fig.5. The test circuit was fabricated using 2um CMOS technology. The inspection opera-
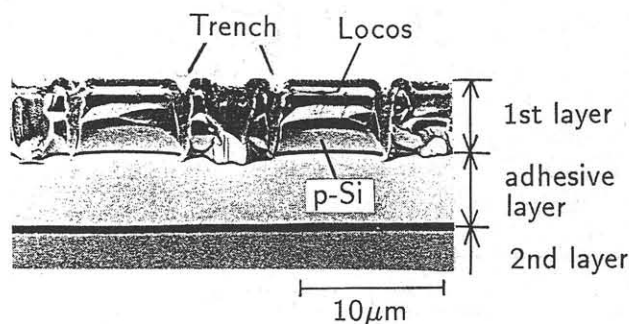
Trench   Locos

1st layer
adhesive layer
2nd layer
p-Si

10μm
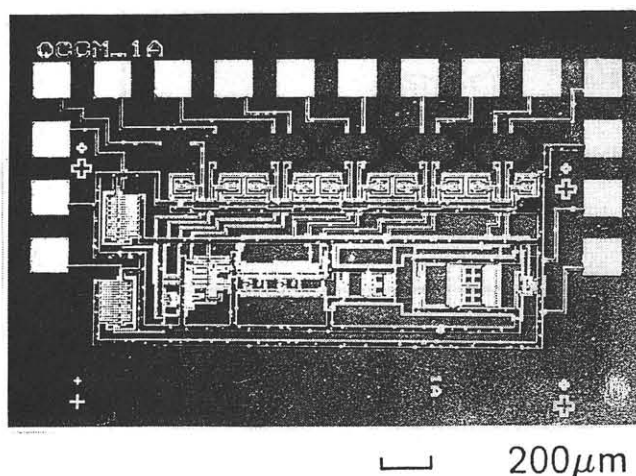
Fig. 4 SEM cross section of 3D structure.

200μm

Fig. 5 SEM micrograph of 3D-OCAM test circuit.

tion among the optical data and the electrical data was evaluated in this test circuit. The waveforms measured in the top layer test circuit are shown in Fig.6. In this operation, the data "1" is electrically written into the flip-flop in the data storage part during the first cycle and the data "0" is optically written into the OC-FF during the second cycle. The electrically written data "1" is simultaneously compared with the optically written data "0" and the data "1" given to the bit lines during the third cycle. The optical match line level becomes low and the electrical match line level becomes high when the matching inspection operation is started by the matching control pulse, because the optically written data "0" is not matched with the electrically written data "1" but the data "1" given to the bit lines is matched with it. Thus, we could confirmed the basic inspection operation of 3D-OCAM. The parallel inspection operation in the vertical direction was examined by the newly developed optical and electrical circuit simulator based on the experimentally confirmed basic operation as shown above. It was found that the parallel data inspection with a block data of 1 Kbit through four memory layers was implemented within 90ns. Thus, the very fast parallel inspection can be achieved by using 3D-OCAM.

5. Conclusion

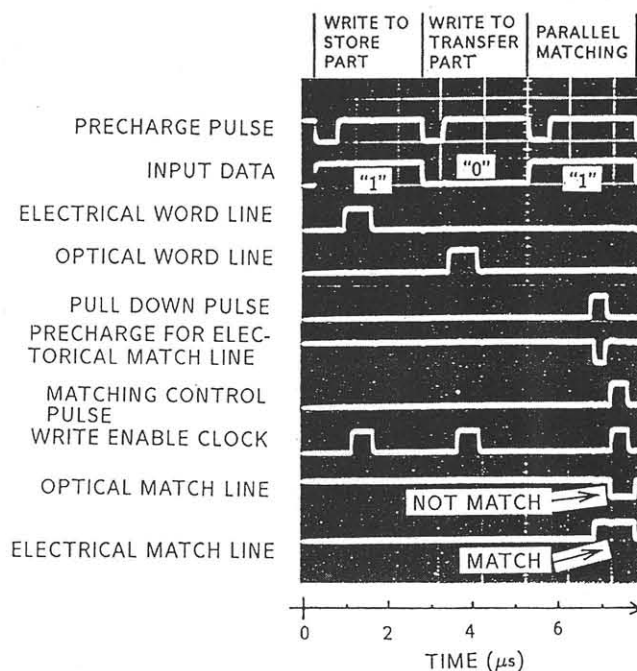The optically coupled three-dimensional content addressable memory (3D-OCAM) was proposed

Fig. 6 Measured waveforms for parallel inspection operation in 3D-OCAM test chip.

for the new parallel processing computer system. The test chip of 3D-OCAM was fabricated and its basic inspection operation was successfully demonstrated.

Acknowledgments

References

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