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Quarter-Micron Interconnection Technologies for 256M DRAMs

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Quarter-micron interconnection technologies for 256 megabit dynamic random access memories (DRAMs) are reviewed. Since the density of memory capacity is increased, both decreasing feature size and increasing sophistication of cell structures are required, resulting in formation of three-dimensional structures. This trend leads us to introduce new interconnection technologies. For plugging quarter-micron contact-holes with high aspect ratios, collimated titanium sputtering and blanket tungsten chemical vapor deposition or aluminum-alloy reflow sputtering would be necessary. For quarter-micron interconnection lines, aluminum-based layered conductor systems or copper metallization would be necessary.

1. INTRODUCTION

Over the past two decades, metal-oxide-semiconductor (MOS) dynamic random access memories (DRAMs) have achieved 256 thousand times increase in density. Since the density of memory cells has been of primary importance in reducing their cost, the reduction in cell size has been achieved not only by the use of smaller line width but also by the increasing sophistication of cell structures and process technologies. As a result, three-dimensional structures have been formed. Therefore, as the minimum feature size has been reduced, the aspect ratios of contact- and via-holes as well as difference in surface level have increased, resulting in poor coverage of the contact and via electrodes and interconnection lines. These problems, associated with interconnections, limit the yield, reliability and performance of the DRAM ultra large scale integrated circuits (ULSIs).

The purpose of this paper is to review the interconnection technologies for 256 megabit (Mb) DRAMs, and discuss the state of the art and current problems for future development.

2. SCALING TREND

As is well known, device feature sizes for MOS DRAMs have been scaled down approximately 67% every generation. Chip sizes of the DRAMs have still increased with increasing memory capacities by a factor of approximately 1.5 every generation although memory cell sizes have been reduced. Figure 1 shows scaling trends of interconnection feature sizes.

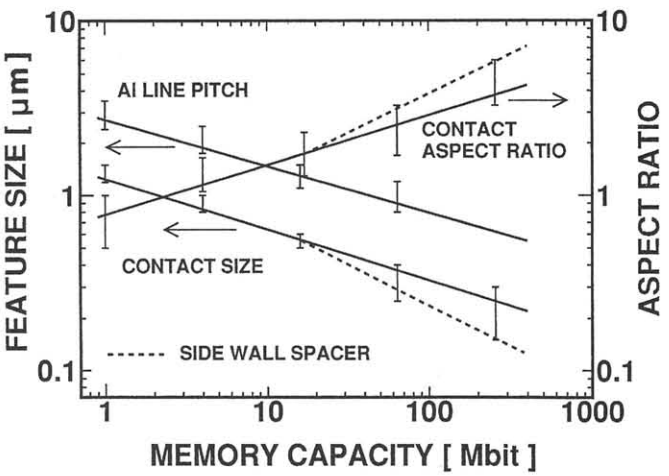

Fig.1. Scaling trends in interconnection feature sizes for DRAMs.

Reduction in interconnection feature sizes has lead to reliability degradations caused by electromigration and stress-induced migration. The increase in wiring resistance as a result of the increase in chip size, has been solved by increasing the number of interconnection levels.

Furthermore, device performance improvement has also been required with reduction in device size. To meet this requirement, the thicknesses of conductors and inter-layer dielectric films have tended to be kept constant to reduce parasitic resistances and capacitances.

This trend has made contact- and via- hole aspect ratios greater than one. Therefore, new contact- and via-hole filling technologies as well as highly reliable multilevel interconnection conductor systems will be necessary.

2.INTERCONNECTIONS IN 256MbDRAM

Figure 2 shows a typical cross section of a 256 Mb DRAM. As can be seen, various contacts and vias with different depths and diameters are necessary due to formation of stacked capacitor cell structures. Various conductor systems are also introduced in the 256 Mb DRAMs as listed in Table 1.

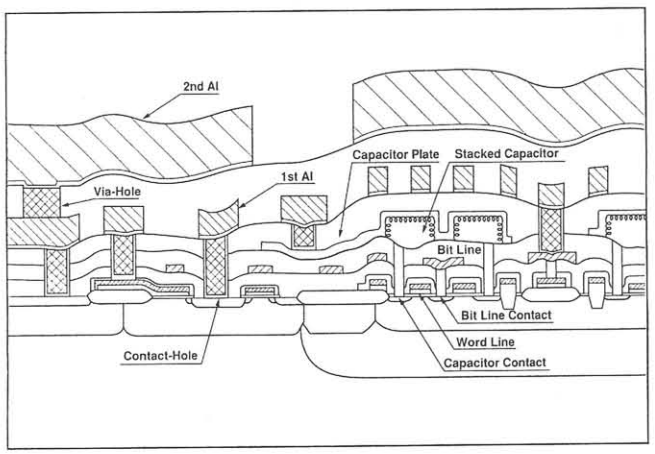

Fig.2. A typical cross section of 256 Mb DRAM.

Table 1 Interconnection Materials and Technologies

INTERCONNECTION	MATERIAL	PROCESS	DESIGN RULE	ASPECT RATIO
Word Line	WSi / Poly-Si	Sputter / LP-CVD	0.25	1 ~ 1.4
Bit Line	WSi	Sputter	0.25	0.5 ~ 1.0
Bit Contact	N+ Poly-Si	Doped LP-CVD	0.25	2 ~ 4
Capacitor Contact	N+ Poly-Si	Doped LP-CVD	0.25	3 ~ 6
Peripheral Contact	W / TiN / Ti	Blanket W-CVD Collimated Sputter	0.3	3 ~ 4
	Al-Ge / TiN / Ti	Reflow Sputter (L.T.) Collimated Sputter		
	Al-Si-Cu / TiN / Ti	Reflow Sputter (H.T.) Collimated Sputter		
Metal Line	TiN / Al-Si-Cu / TiN / Al-Si-Cu / TiN	Sputter	0.25	1 ~ 2
	Cu	Sputter		
Via-Hole	W / TiN / Ti	Blanket W-CVD Reactive Sputter	0.6	1 ~ 1.5
	Al-Ge / TiN / Ti	Reflow Sputter (L.T.) Reactive Sputter		

Contact holes of minimum geometries on the order of 0.25 μm and aspect ratio greater than one must be plugged with an interconnection material having good coverage, low resistivity, stability during thermal processing, and compatibility with existing processes.

For plugging high-aspect-ratio, quarter-micron contact-holes with doped polysilicon the multiple layer method is necessary to insure the stable configuration with high dopant concentration, large grains, and smooth , uniform morphology for contact-hole coverage[1].

In order to achieve lower contact resistances in high aspect ratio contact-holes, metal plugging is necessary. Chemical vapor deposition (CVD) metal technologies, which have good contact coverages, have been developed. Conformal metal films are needed to fill the contacts with high aspect ratios. Therefore, blanket tungsten (W) CVD is introduced for filling contact-holes. Conventionally, H_2 reduction of WF_6 has been used for blanket CVD because it provides conformal W films. A contact hole with 0.25 μm diameter and 1 μm depth can be filled by blanket W-CVD. In addition, Al-CVD[2] or Copper (Cu) CVD[3] and titanium nitride (TiN) CVD may also be introduced.

On the other hand, physical sputtering of titanium (Ti) is still indispensable to reduce contact resistance, in spite of its poor step coverage. Collimated sputtering technology has been developed to improve the contact coverage. A collimator , whose aspect ratio is 1.0, is placed between the sputter target and the wafer so that the wafer can collect the fraction of Ti clusters with normal incidence angle to the surface of the wafer. Figure 3 shows a cross section SEM micrograph showing collimated Ti step coverage in a quarter-micron contact hole.

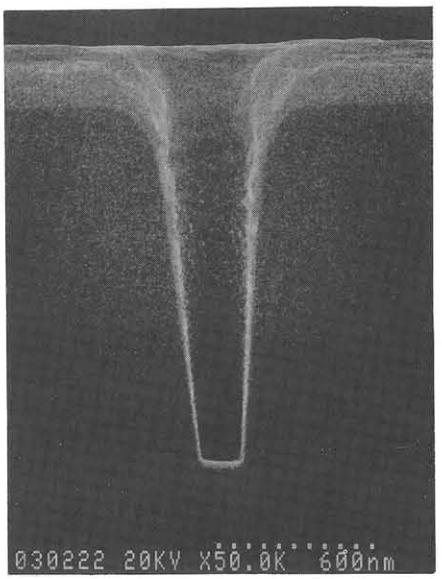

Fig.3. A cross section SEM micrograph of Ti deposited by collimated sputtering.

Aluminum (Al) alloy reflow sputtering is also a promising technology for contact-hole filling in terms of reducing fabrication cost. Aluminum-germanium (Al-Ge) alloy[4] can flow and fill in quarter-micron contact holes at 300°C, as shown in Fig. 4, because of its lower eutectic temperature (424°C) than other Al-alloys.

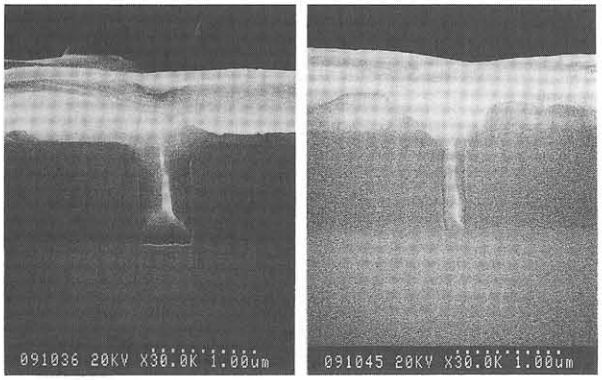

Fig.4 Cross section SEM micrographs of Al-Ge electrodes reflow-sputtered at 300°C.

Figure 5 shows a SEM micrograph of Al lines in 256 Mb DRAM. As interconnection dimensions are reduced to 0.25 μm, new fabrication processes are required[5]. Furthermore, reliability failures due to electromigration and stress-induced migration become more serious for conventional Al conductors. Pure-Cu may be introduced as an interconnection material[6]. Still, further development of aluminum-based technologies for quarter-micron interconnections should be continued.

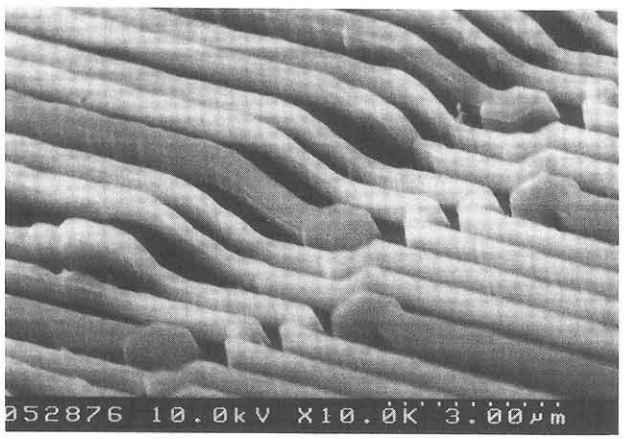

Fig.5. A SEM micrograph of Al lines in 256 Mb DRAM.

A new interconnection structure using TiN/Al-1%Si-0.5%Cu/TiN/Al-1%Si-0.5%Cu/TiN/Ti layered films has been developed for both electro- and stress-migration-resistant interconnections[7] as shown in Fig.6. The multilayer interconnection shows larger Vickers hardness value, less tensile stress relaxation and longer electromigration lifetime in comparison with Al-Si-Cu single layer. These improvements are due to the rigid intermetallic compounds, Ti_xAl_y at the interface between TiN and Al-Si-Cu.

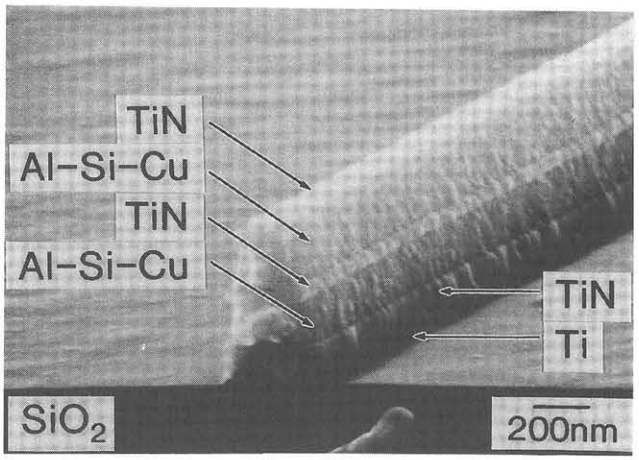

Fig.6. A SEM micrograph of a quarter-micron TiN/Al-Si-Cu/TiN/Al-Si-Cu/TiN/Ti multilayer interconnection.

3. SUMMARY

Quarter-micron interconnection technologies for 256 Mb DRAMs are reviewed. For quarter-micron contact-hole plugging, collimated Ti sputtering and blanket W-CVD or Al-alloy reflow sputtering would be necessary. For quarter-micron interconnection lines, Al-based layered conductor systems or Cu metallization would be necessary.

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