# Low Resistance and Thermally Stable Ti-Silicided Shallow Junction Formed by Advanced 2-Step Rapid Thermal Processing and Its Application to Deep Submicron Contact

H.Kotaki, K.Mitsuhashi, J.Takagi, Y.Akagi\*, and M.Koba\*

Central Research Laboratories, Research and Analysis Center\*, Sharp Corporation 2613-1, Ichinomoto-cho, Tenri-shi, Nara 632, Japan

A low resistivity thermally stable TiSi<sub>2</sub> shallow junction applicable to a deep submicron contact has been developed. This was achieved through the use of an advanced 2-step rapid thermal silicidation called the "AAS" process and the use of an Al-based metal / TiN / Ti / TiSi<sub>2</sub> contact technique. The low sheet resistance and high thermal stability of TiSi<sub>2</sub> films on n<sup>+</sup>-Si reached the same level as that on undoped Si, though silicidation on n<sup>+</sup>-Si is more difficult than that on p<sup>+</sup> or undoped Si. The film and contact resistivities were about 11.5 $\mu\Omega$ cm and 1~2x10<sup>-8</sup> $\Omega$ cm<sup>2</sup>, respectively. Ring oscillators using these processes exhibited a 15% improvement in speed as compared with conventional cases (without SALICIDE).

## INTRODUCTION

As a means of ultimately overcoming the problems involved in increasing sheet resistances of transistor source and drain, and contact resistances in deep submicron ULSI, the research and development of a self-aligned silicide (SALICIDE) technique<sup>(1-3)</sup> is now progressing rapidly. In the</sup> SALICIDE process, TiSi2 film is becoming widely used because of its low resistivity<sup>(4)</sup>. However, it is quite difficult to form the TiSi2 layer with low resistance on n+-Si as compared to that on p<sup>+</sup> or undoped Si<sup>(5)</sup>. The probable causes of this are the difference in the crystal structure and formation rate of the TiSi<sub>2</sub> layer on n<sup>+</sup> and p<sup>+</sup>-Si substrates. For this reason, optimization of the TiSi2 formation process was investigated by studying 75As+ doping into the substrate before silicidation (ABS process) and after silicidation (AAS process). Furthermore, Ti has the property of decomposing the oxide<sup>(6)</sup>. Taking advantage of this property, a contact technique using Al-based metal / TiN / Ti interconnection on TiSi2 was employed. These techniques (AAS process and Albased metal / TiN / Ti / TiSi2 contact technique) were more applicable to transistor devices which require lower source and drain resistances and shallower junctions for higher speed operation.

### EXPERIMENTAL

The process flows of the AAS and ABS processes are shown in Fig.1. In both processes, the Ti films with 50nm thickness were deposited by an ultra high vacuum DC magnetron sputtering system, of which the base pressure was lower than  $3x10^{-9}$  Torr. The self-aligned silicide (SALICIDE) process employed a 2-step Rapid Thermal Annealing (RTA) with halogen lamp heating<sup>(7)</sup> in a N<sub>2</sub> atmosphere. After the first low temperature RTA process, the TiN and unreacted Ti were etched off by a H<sub>2</sub>SO<sub>4</sub> based solution, followed by second high temperature RTA for the final silicidation. The formation of n<sup>+</sup> junction for ABS process was performed by  $^{75}As^+$  implantation at 40keV with a dose of 5E15cm<sup>-2</sup> and subsequent furnace annealing at 900°C for 20 minutes in a N<sub>2</sub> atmosphere. For the AAS process,  $^{75}As^+$  implantation into silicide layer was performed between the two RTA steps, and second RTA was then carried out for dopant drive and final silicidation simultaneously. The TiSi<sub>2</sub> film properties were examined by using a four-point probe method, transmission electron microscopy (TEM) and X-ray diffraction (XD).

LDD-NMOSFETs with gate oxide of 9.7nm-thick and gate side wall oxide of 200nm-thick were formed on p-type (100) oriented substrate using the optimized AAS process. Except for the silicidation and metallization processes, the fabrication processes are substantially the same as the conventional processes. After silicidation using the AAS process, the metallization process was performed with Albased metal (500nm) / TiN (150nm) / Ti (70nm) tri-layered structure. In advanced of this aluminum metallization process, Ti and TiN were sequentially sputtered on TiSi2 films, and then the RTA (750°C, N2, 20sec) process was performed to decompose the contact bottom oxide by Ti atoms. The diameter of contact sizes which were measured by scanning electron microscopy ranged from 0.35 to 1.0µm. The contact resistances were investigated using the Kelvin method. The performance of the NMOSFETs were estimated by measuring the propagation delay time (tpd) of a 37 stage Ring Oscillator with an E-E inverter circuit (W=5.0/1.5µm: Driver/Load, VD=3.3V).

### **RESULTS AND DISCUSSION**

Figure 2 shows sheet resistances of the TiSi<sub>2</sub> film and

their uniformities on undoped Si as a function of the first RTA temperature before and after the second RTA at 850 °C. One notes that the sheet resistances decreased drastically by performing the second RTA. Uniformities of the TiSi<sub>2</sub> film sheet resistance were not degraded by the second RTA. This result indicates that the variation of the TiSi<sub>2</sub> film sheet resistance is due to the variation of TiSi<sub>2</sub> film thickness and not to the variation of the film quality. In the samples after the second RTA, formation of the perfect C54 TiSi<sub>2</sub> phase structure was confirmed by XD spectra and TEM.

Figures 3(a) and 3(b) show the dependence of the TiSi2 film sheet resistance on the first RTA and second RTA temperature, respectively. Here, the method of the n+ doping was studied by comparing the AAS and ABS process with undoped process. The AAS process achieved excellent film properties, and the sheet resistances were almost equal to the silicidation of undoped Si after the second RTA in the temperature range between 850 °C and 1050 °C. On the other hand, with the ABS process, the sheet resistances were substantially larger than the other process. The large sheet resistance at the first RTA temperature of 600°C indicates that the As atom occurs the delay of the silicidation. In addition, the sudden increase of the sheet resistance at the second RTA temperature of 1000 °C suggests that the TiSi2 film formed by the ABS process tends to agglomerate at lower temperature as compared to that by the other process. In the XD patterns for the samples formed by the AAS or undoped process, only d=0.230nm peak, attributed to the (311) reflection of the TiSi<sub>2</sub>-C54 phase, was confirmed. In the samples formed by ABS, two peaks at d=0.230nm and 0.214nm were observed. The peak at d=0.214nm was probably the (040) reflection of the TiSi<sub>2</sub>-C54 phase (d=0.2138nm). Differences in the TiSi<sub>2</sub> / Si interface area between the AAS and the ABS processes were observed by TEM micrographs, as shown in Fig.4. The TiSi2 / Si interface formed by the AAS process was quite smooth. However, in the TiSi2 / Si interface of the ABS process, Moire fringes were observed. It is considered that these two peaks (d=0.230nm, 0.214nm) appeared as a result of the Moire fringes. Also, TEM micrographs showed that the TiSi2 film thicknesses formed by the AAS and ABS processes under the first RTA condition of 625°C N2 20sec were about 50 and 40nm, respectively. At these TiSi2 film thicknesses, the resistivities of these TiSi2 films formed by the AAS and ABS were calculated at about  $11.5\mu\Omega cm$  (2.30 $\Omega$ /square at 50nm) and  $15.3\mu\Omega cm$  ( $3.82\Omega/square$  at 40nm), respectively. A very thin, low-resistive, and thermally stable TiSi<sub>2</sub> film on n<sup>+</sup> (As<sup>+</sup>) doped Si could be obtained using the AAS process.

Figure 5 shows the dependence of the contact resistance on contact diameter in the Al-based metal / TiN / Ti / TiSi<sub>2</sub> structure using the AAS process and the conventional Al-based metal / TiN / Ti structure, respectively. In the Al-based metal / TiN / Ti / TiSi<sub>2</sub> structure, contact resistances of one order of magnitude lower than the conventional case were obtained. These contact resistivities were about  $1\sim 2x10^{-8}\Omega cm^2$  for the diameter from 1.0µm to 0.35µm. With the AAS SALICIDE and Al-based metal / TiN / Ti / TiSi<sub>2</sub> contact technique, contact resistance of 22  $\Omega$  for 0.35µm diameter (0.096µm<sup>2</sup> contact area) was achieved.

Figure 6 shows the ID-VD characteristics of SALICIDE NMOSFET with a physical gate length of 0.4µm and gate oxide thickness of 9.7nm formed by using the AAS process and Al-based metal / TiN / Ti / TiSi2 structure. It was confirmed that high drivability and good properties were The for the NMOSFETs. maximum achieved transconductance in linear region was about 32.9µS/µm. Furthermore, these SALICIDE NMOSFETs circuits were faster than conventional (without SALICIDE) NMOSFETs circuits by about 15%, as shown in Fig 7. This was estimated by measuring the propagation delay time (tpd) of a 37 stage Ring Oscillator with an E-E inverter circuit (W=5.0/1.5µm: Driver/Load, VD=3.3V).

## CONCLUSIONS

A method of silicidation on n+-Si, which is more difficult than that on p<sup>+</sup> or undoped Si, has been developed. By using the AAS process, a very thin, low-resistive, and thermally stable TiSi2 film on n+ (As+) doped Si could be obtained. The resistivity of this film was about  $11.5\mu\Omega cm$ . Furthermore, using the Al-based metal / TiN / Ti / TiSi2 structure contacts technology, the specific contact resistivities were about 1~2x10<sup>-8</sup>Ωcm<sup>2</sup>. NMOSFETs with the Ti silicide fabricated by the AAS process and Al-based metal / TiN / Ti / TiSi2 structure contact technology have demonstrated excellent The maximum transconductance in linear characteristics. region was about 32.9µS/µm with physical gate length of 0.4µm and gate oxide thickness of 9.7nm. These SALICIDE NMOSFETs were faster than conventional (without SALICIDE) NMOSFETs by about 15%, estimating the tpd of a 37 stage Ring Oscillator with an E-E inverter circuit (W=5.0/1.5µm: Driver/Load, VD=3.3V). This technology can be expected to become important for the development of future deep submicron devices.

#### ACKNOWLEDGMENTS

The authors would like to thank the staff of VLSI Development Laboratories, Research and Analysis Center and Central Research Laboratories, Sharp Corporation, for helpful discussion and their cooperation in fabricating samples.

#### REFERENCES

- (1) T.Shibata et al., IEDM Tech. Digest, 647 (1981)
- (2) C.Y.Ting et al., ECS Proc. 1st Int. Symp. on VLSI Science and Technol., 224 (1982)
- (3) C.M.Osburn et al., ECS Proc. 1st Int. Symp. on VLSI Science and Technol., 213 (1982)
- (4) S.P.Murarka: Silicides for VLSI Applications, Academic press: p.30-31 (1983)
- (5) D.Moy et al., ECS Proc. 1st Int. Symp. on VLSI Science and Technol., 381 (1987)
- (6) R.Beyers, J. Appl. Phys. 56, 147 (1984)
- (7) K.Tsukamoto et al., Ext. Abst. 16th Int. Conf. on Solid State Devices & Mat., 47 (1984)

