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A Proposal of Self-Learning Neuron Circuits with High-Density Synapse Connections of Ferroelectric Thin Films

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1. Introduction

In future neural networks, it is highly desirable that the weight function of the synapse connections in neuron circuits is changed through self-learning process. In this paper, the term of "self-learning" is defined as a function in which electrical or optical properties of a device are changed partially or totally after the device has processed a certain number of usual signals, and self-learning neuron circuits with excitatory and inhibitory synapses are proposed. The self-learning function is different from degradation of the device, since the properties can be restored to the initial state by initiallized signals.

2. Self-Learning MISFETs

A key component to realize the self-learning function is a MISFET with a ferroelectric gate insulator film as shown in Fig.1. Proposals of such structures are old [1] and fairly good results have been reported very recently[2]. In these applications, in order to change the source-drain resistance or the drain current of FET, control pulses higher than usual signal pulses are applied to the gate electrode for changing the polarization of the film. On the other hand, in the self-learning MISFET, the ferroelectric film thickness is so chosen that the polarization of the film is gradually changed by applying signal pulses. As a result, an initially normally-on FET changes to a normally-off FET and vice versa. The device structure can easily be designed by using the switching characteristics of ferroelectric films [3]. An example of the design is shown in Fig.2, in which "number of learning times" means the number of pulses which change the Si surface of a MIS diode to an inversion state[4].

3. Neuron Circuits

The self-learning MISFETs seem to fit to analog circuits better, since the threshold voltage or the source-drain resistance of the FET changes gradually by applying signal pulses. In order to combine two concepts of the analog output and the pulse input to the self-learning FET, I propose to use a PFM(pulse frequency modulation) system, in which asynchronous short pulses are generated just as current pulses through nerve membrance in a human brain.However, this system is somewhat different from the synchronized pulse density neural system[5].

A basic circuit of the pulse generator is shown in Fig.3, which is known as a trigger circuit of a thyristor. In this circuit, a UJT (unijunction transistor) is used as a switch to discharge the capacitance C, and the pulse interval is proportional to CR_1. Therefore, if R_1 is replaced by the source-drain resistance of the self-learning FET, it is possible to change the output pulse interval of the neuron circuit. Since the UJT is a positive feedback device, it is necessary that the neuron circuit is fabricated in the SOI (Si-on-insulator) structure and each device is electrically isolated so that the circuit is not latched-up.

In order to change the output pulse interval in both shorter and longer directions,the gate input signals with positive and negative polarities are necessary. This function can be interpreted such that the neuron circuit has both of the excitatory and inhibitory synapses. The proposed circuits are shown in Figs.4 (a) and (b), in which optical and electrical connections between neurons are used.

Finally, I propose the design of the multiple-input neuron circuits and the layout of the synapse connection. Figure 5 shows an optically-connected n-neuron array, in which each neuron has m synapses and they are fully connected to the previous array of m neurons. In this array, the self-learning FETs in each neuron are connected in parallel so that the output pulse interval is determined by the time constant of C $\times$(total resistance).

The layout of the synapse connection is shown in Fig.6, in which Si stripes with a lateral npn structure are placed on an insulating substrate, they are covered with a ferroelectric film, and the metal stripes for the gate electrodes are placed on the film with a right angle to the Si stripes. In order to give the initial weight of respective synapses independently, a pulse bias voltage of $+V_0/2$ and a DC bias of $-V_0/2$ are applied to the selected metal and Si stripes, respectively, so that the voltage difference V_0 exceeds the critical value for polarization only at the cross point and the weight can be adjusted by changing pulse duration.

Since the synapse circuit has no via-hole as shown in Fig.6, the packing density of synapses is expected to be very high. Actually, the synapse area designed by a 1μm rule is about $4\times2\mu m^2$. (3μm-wide Si stripes, 1μm-wide metal stripes and 1μm-wide spaces) Since the area of each neuron circuit is not large, the area for 1000 neurons with 1 M total synapses is expected to be about $8mm^2$. This area is considered to be small enough compared to other neural networks.

4. Summary

Novel self-learning neuron circuits are proposed. Main features are (1) self-learning MISFETs with ferroelectric gate insulators, (2) asynchronous PFM outputs, (3) excitatory and inhibitory synapses, (4) high-density synapse layout, (5) independent determination of the initial weight of synapses, and (6) optical and electrical connections between neurons.

[References]

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2) T.A.Rost et al: APL, 59, 3654 (1991)
3) J.F.Scott et al: JAP, 64, 787 (1988)
4) H.Ishiwara et al: Gekkan Semiconductor World, 11, 98 (Jan. 1992) (in Japanese)
5) H.Eguchi et al:Trans.IEICE J74-C2,369 (91)

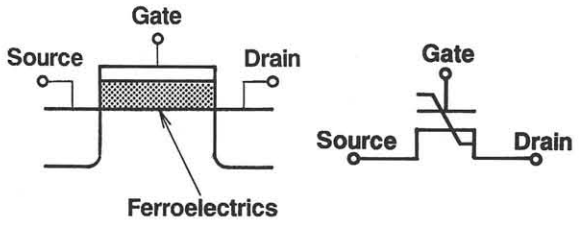

Fig.1

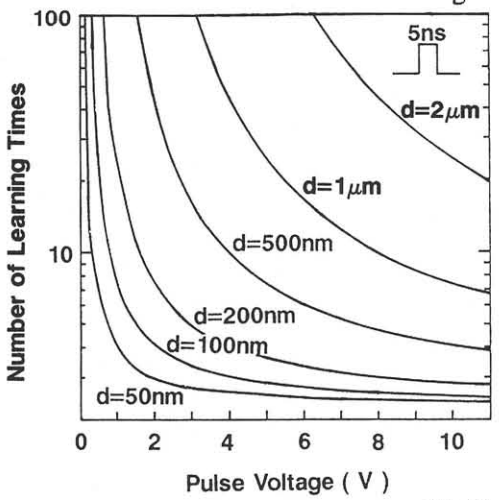

Fig.2

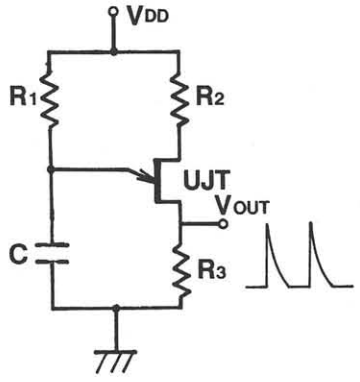

Fig.3

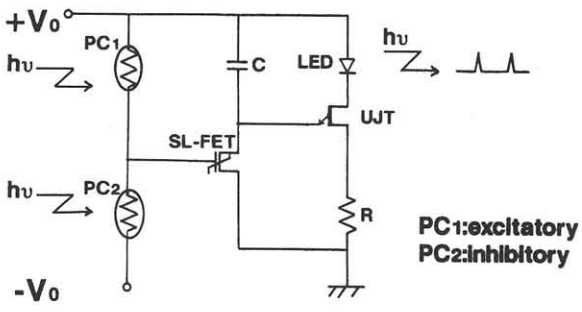

Fig.4 (a)

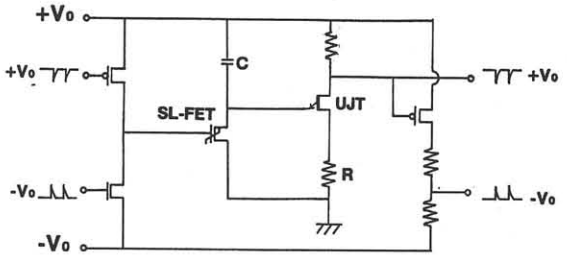

Fig.4 (b)

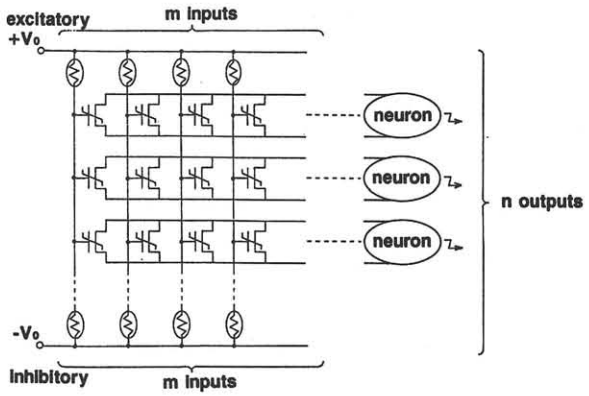

Fig.5

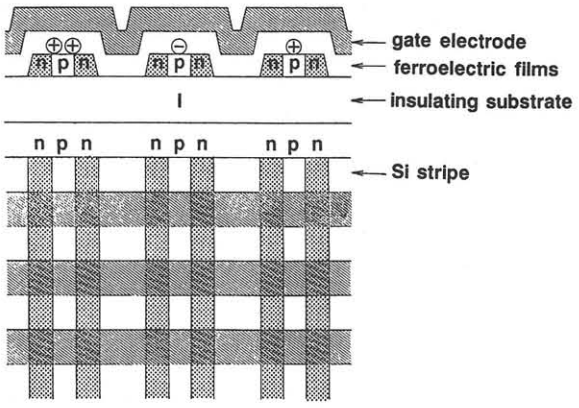

Fig.6