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A Novel Fabrication Method for Poly-Si TFTs with a Self-Aligned LDD Structure

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In active matrix liquid crystal displays using poly-Si TFTs, one of the main subjects is to decrease their OFF currents(1). Poly-Si TFTs with a lightly doped drain(LDD) structure have been widely investigated(2). However, it has a drawback of requirements of an additional photo-mask and precise mask alignment.

In order to solve these problems, we have developed a novel fabrication method for poly-Si TFTs with a self-aligned LDD structure. Our method is applied a lateral etching of n^+ Si film to make a LDD region. The lateral etching is caused by dry etching in patterning process of gate electrode. The method makes it possible to realize the self-aligned LDD structure by a simple process and it results in poly-Si TFTs with a high ON/OFF ratio.

The poly-Si TFTs were fabricated on a quartz substrate. A 100nm thick amorphous Si film, deposited by LPCVD at 480 °C using Si_2H_6 gas, was crystallized at 625 °C for 6 h. A poly-Si film with a relatively large grain size of 1-2 μm was obtained. A 72nm thick gate oxide was formed by thermal oxidation at 950 °C. In order to realize the self-aligned LDD structure, the following novel process was employed. First, after a photo-resist for the gate electrode was formed on a 300nm thick n^+ Si film, the n^+ Si film was etched using SF_6 gas by a reactive ion etching (RIE) method. The conditions of the RIE were an RF power of 200W and a gas pressure of 40 mTorr. Since SF_6 gas results in isotropic etching, a lateral etching of the n^+ Si film occurs under the photo-resist by an over etching (undercut) (Fig.1-(a)). Second, P^+ ions were implanted at a dose of 1.5×10^{15} cm^{-2} to form the source and drain using the photo-resist as a mask(Fig.1-(b)). Next, the photo-resist was removed and the second ion implantation at a dose of 2×10^{13} cm^{-2} was followed to make the LDD region (Fig.1-(c)). The above-mentioned novel process results in the self-aligned LDD structure. The source/drain electrodes were fabricated with Cr/Al metals and hydrogenation was performed efficiently using an ECR plasma process.

Fig.2 shows dependence of the undercut length (ΔL) on the over etching time. Here, the over etching time was counted from an end point of the dry etching of n^+ Si films. The end point was detected by plasma emission of F^* (704nm). The undercut by the lateral etching of n^+ Si film was confirmed by SEM. As shown in the figure, the ΔL is proportional to the over etching time. It is concluded that the ΔL, which is equal to LDD length, can be precisely controlled by the over etching time.

Fig.3 indicates the dependence of drain current on the gate voltage (Vg) as a function of the ΔL. At the ΔL=0μm, the field effect mobility of the poly-Si TFT is as high as $80cm^2/V \cdot s$ and the OFF current at Vg=-5V is about 10^{-11}A. Adoption of our LDD structure with ΔL>1.4μm decreases the OFF current at a reverse bias by more than one order of magnitude, as shown in the figure. At this time, a drastic decrease of the ON current and a significant decrease of the sub-threshold slope are not observed until the ΔL reaches 3.4μm. Fig.4 shows the OFF current (`Ioff`) at Vg=-5V and the ON current (`Ion`) at Vg=20V as a function of the ΔL. The `Ion` is an almost constant for ΔL < 2.5μm. On the other hand, the `Ioff` has an almost constant value as low as 10^{-12} A in the range of 1.4μm <ΔL< 3.3μm. Therefore, it is concluded that the range of 1.4μm <ΔL < 2.5μm is at least effective to realize poly-Si TFTs with a high ON current and a low OFF current. As shown in Fig.2, our novel fabrication method has a time tolerance (about 90 s) enough to control the ΔL from 1.4μm to 2.5μm. Then, this method gives us high reproducibility for fabricating such a self-aligned LDD structure.

In conclusion, we have succeeded to develop a novel process for the self-aligned LDD structure, which leads to the decrease of the OFF current by more than one order of magnitude without an additional photo-mask process.

REFERENCES

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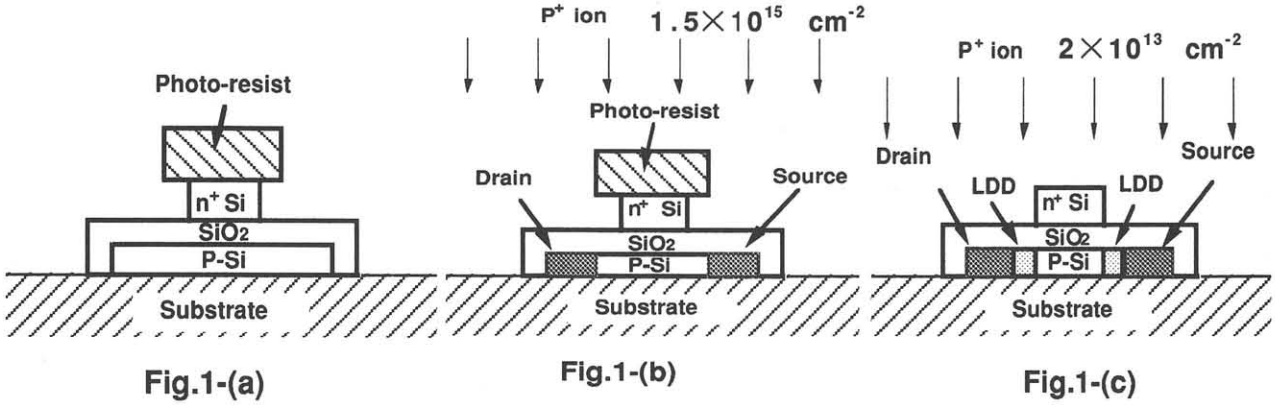

Fig.1-(a) Fig.1-(b) Fig.1-(c)

Fig.1 A novel fabrication process for poly-Si TFTs with a self-aligned LDD structure.

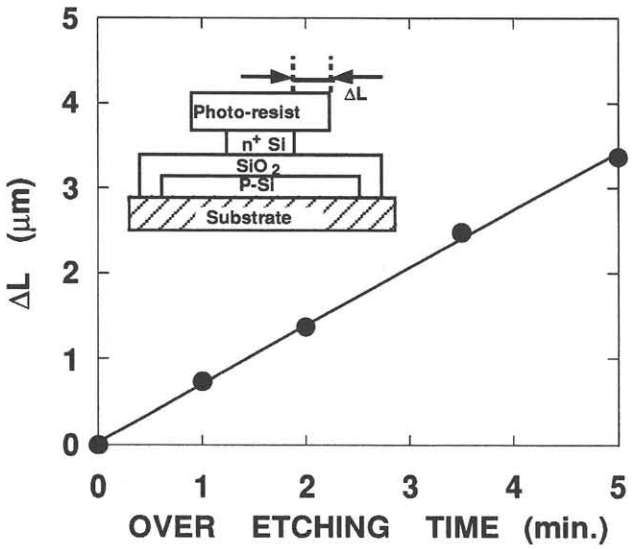

Fig.2 Dependence of undercut length(ΔL) on over etching time.

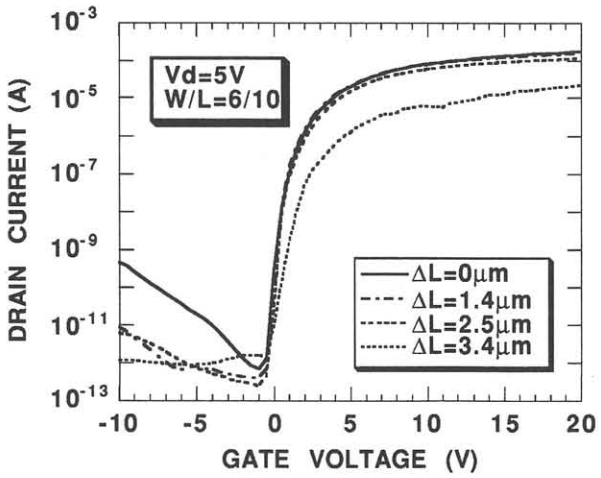

Fig.3 Dependence of drain current on gate voltage as a function of ΔL at a drain voltage (Vd) of 5V.

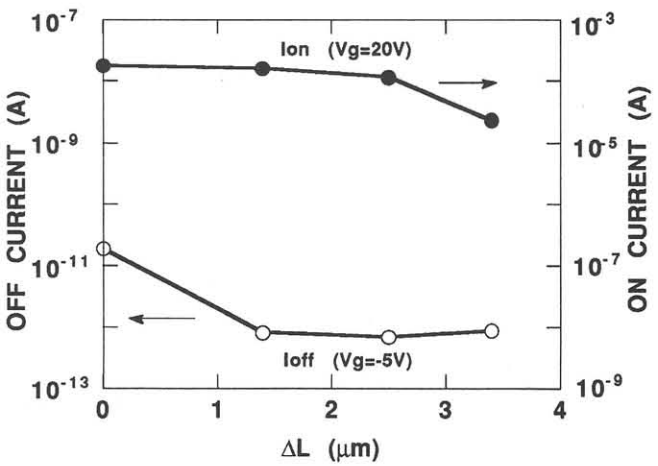

Fig.4 ON and OFF currents as a function of ΔL.