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Low Voltage, High Gain, 0.2μm NMOSFETs by Channel Counter Doping with As

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One of the most serious problem in sub half micron MOS devices is to reduce the short channel effect and realize stable threshold voltage (Vth) control [1,2]. Among the technological trends in MOS ULSIs, low voltage operation is one of the most important issues, and requires a lower Vth characteristic. The above two subjects, smaller channel length and lower threshold voltage are, however, generally incompatible, in terms of substrate impurity concentration [3]. Thus, it is getting more difficult to miniaturize MOS devices with a low Vth characteristic, down to the deep sub micron regime. In this paper, a Vth control method by counter channel doping with arsenic is investigated and its feasibility in realizing 0.2μm NMOS transistors with Vth of 0.3V, is demonstrated. The high current drivability of this transistor is also discussed.

Devices used in this study were n^+ poly gate NMOSFETs, with a gate oxide thickness of 6nm and a conventional single drain structure. A boron implant, forming a punchthrough stopper, and an arsenic implant for threshold adjustment, were done through a sacrificial oxide. The temperature during the thermal cycle after source/drain implantation (As^+, $2x10^{15}cm^{-2}$, 30keV) was 850°C or below. Fig.1 shows the channel substrate doping profile for NMOSFETs used in this work. Fig.1(a) and (b) show profiles for conventional devices, while (c) shows the counter-doped type transistor (CD-MOSFET) profile, proposed here. Fig.1(a) has a higher boron concentration in order to reduce punchthrough, while (b) has a lower doping level to achieve a lower Vth. In the case of the CD-MOSFET, arsenic was implanted to the surface of the substrate which had the same boron impurity profile as (a). The cross section of this transistor is illustrated in Fig.2. The device simulator CADDETH was used to perform 2D-device simulation, particularly for the electric field analysis in the devices.

Fig.3 shows the threshold voltage dependence on the effective channel length (L_{eff}) for the three transistors, having substrate doping profiles shown in Fig.1. Although (a) has a better short channel characteristic than (b), its Vth is higher. In the case of (b), Vth is lower, but Vth fall-off occures at longer L_{eff}. This is simply because the lower punchthrough stopper concentration for low Vth accelerates the short channel effect. The CD-MOSFET shows Vth as low as (b), while keeping short channel behaviour as good as (a). The correlations between Vth and minimum effective channel length ($L_{eff,min}$) before the onset of the short channel effect are shown in Fig.4. $L_{eff,min}$ is defined as the channel length where the change in Vth against L_{eff} reaches a critical value. (*i.e.* $\Delta Vth/\Delta L_{eff}$=0.1V/0.1μm) From this figure, lower Vth is found to cause worse short channel effect, for the conventional transistor, while for the CD-MOSFET, Vth adjustment can be done without losing good short channel characteristics.

Fig.5 shows the dependence of the reciprocal of the transconductance on the gate length for two kinds of transistors which have substrate doping profiles shown in Fig.1 (a) and (c) respectively, both having equivalent short channel behaviour. From these data, electron mobility of the CD-MOSFET was estimated to be 304 cm^2/Vsec, which was larger than that of the conventional one (233 cm^2/Vsec) by 30%. Fig.6 shows the Id vs. Vd characteristic of CD-MOSFET. Impurity concentration at the surface of the CD-MOSFET, where the channel is formed, is apparently much higher than that of the conventional one. Thus, impurity scattering is expected to be larger in the CD-MOSFET, which is inconsistent with its higher carrier mobility. Fig.7 shows the simulated vertical electric field (Ez) at the surface, for which the bias condition was Vg=1.5V with grounded source, drain and substrate. In the conventional MOSFET, Ez was 0.56MV/cm, which is 1.8 times larger than that in the CD-MOSFET. This means that surface scattering in the CD-MOSFET is smaller. The above analysis shows that the higher electron mobility in the CD-MOSFET can be attributed to reduced vertical electric field at the surface, resulting in smaller surface scattering. Also, the electron mobility is dominated by surface scattering rather than impurity scattering.

In conclusion, the CD-MOSFET, whose Vth is controlled by counter doping, can be a solution in realizing sub-half micron devices with low threshold voltage. The CD-MOSFET also has the advantage of higher carrier mobility.

References

[1] G.A.Sai-Halasz et al., IEEE EDL, 38, 463 (1987)
[2] S.Kimura et al., IEDM Tech. Dig., 950 (1991)
[3] W.Fichtner et al., IEDM Tech. Dig., 722 (1982)

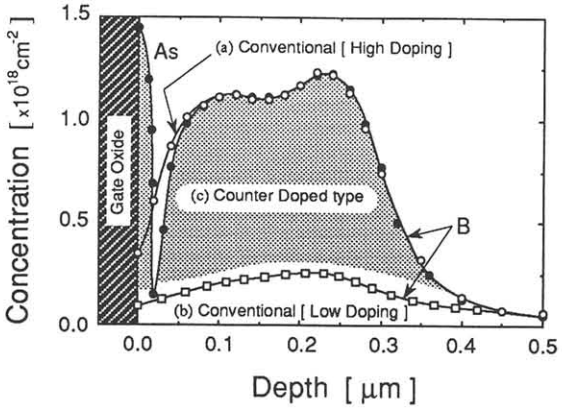


Fig.1 Impurity profiles

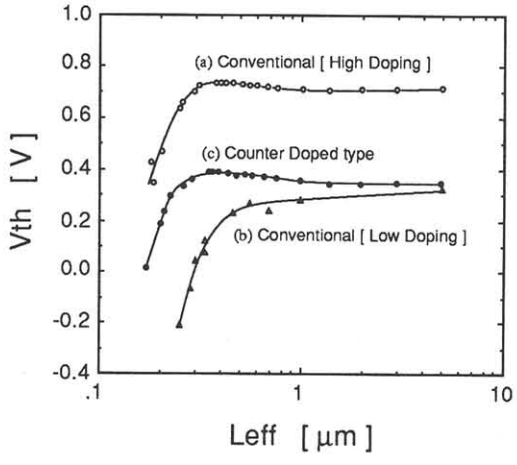


Fig.3 Threshold voltage dependence on Effective channel length

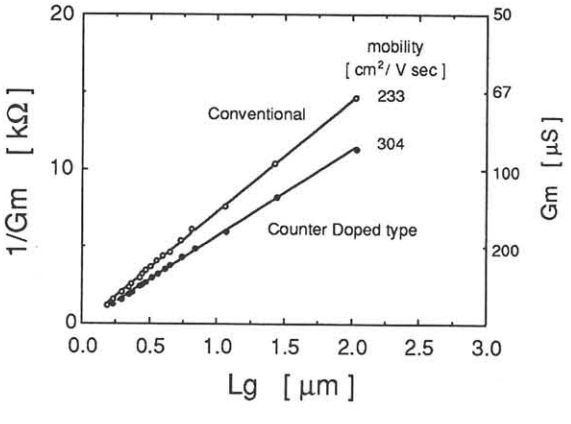
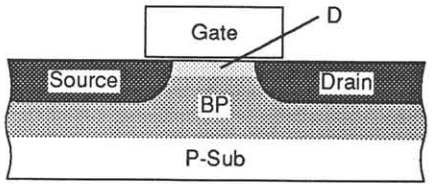


Fig.5 Relation of reciprocal of transconductance vs. gate length



D : Counter doped region (As)
BP : Punchthrough stopper (B)

Fig.2 Counter doped NMOSFET

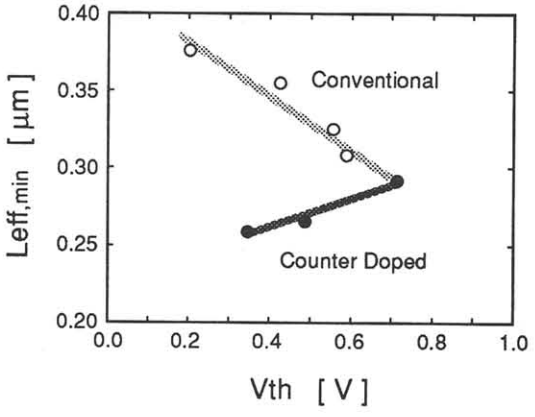


Fig.4 Correlation between threshold voltage and minimum effective channel length
($L_{eff,min}$: @ $\Delta Vth / \Delta L_{eff} = 0.1V / 0.1\mu m$)

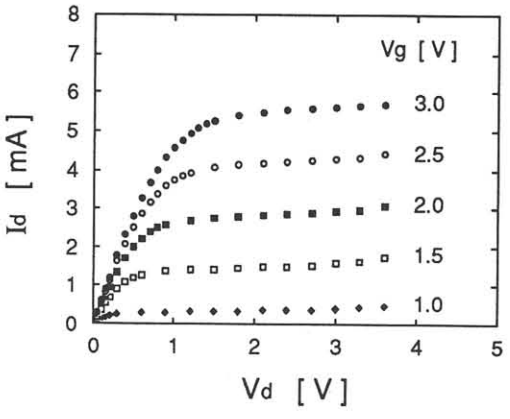


Fig.6 Id vs Vd characteristic of counter doped NMOSFET
Leff=0.25μm, W=10μm

	Vertical Electric Field : Ez
Counter Doped	3.2 x 10^5 [V / cm]
Conventional	5.6 x 10^5 [V / cm]

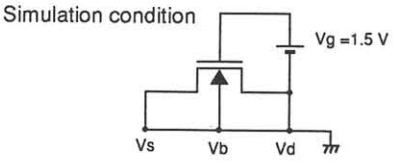


Fig.7 Simulation of vertical electric field at the Si surface