Extended Abstracts of the 1992 International Conference on Solid State Devices and Materials, Tsukuba, 1992, pp. 697-698

Ultrathin Ta_2O_5 Films on Rapid Thermal Nitrided Rugged Polysilicon for High Density DRAMs

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For 64 and 256 Mb DRAM memory chips, Ta_2O_5 films [1, 2] or ON films on rugged polysilicon bottom electrodes [3-5], have been proposed recently and were shown to give capacitance values higher than 10 fF/μm^2. Until now, Ta_2O_5 films have been studied only on smooth electrodes [1, 2]. This paper demonstrates for the first time to combine Ta_2O_5 films with rugged bottom capacitor electrodes to maximize the capacitance per unit area. The electrical properties of these structures are also presented.

Planar capacitors shown in Fig. 1 are fabricated on 150-mm (100), p-type Si wafers covered with a 200-nm-thick SiO_2 layer. The bottom 100-nm-thick polysilicon electrode is deposited by LPCVD at 80 mTorr. Films deposited at 625°C will be referred to as "smooth", while layers deposited at 550°C will be referred to as "rugged" [3, 4]. The smooth and rugged polysilicon surfaces are then PH_3-doped at 860°C and treated by rapid thermal nitridation (RTN) in pure NH_3 at 950°C for 30 sec. This treatment is required to maximize the film storage efficiency by preventing the formation of an interfacial SiO_2 layer during the subsequent Ta_2O_5 oxidation step [2]. 10 and 15-nm-thick Ta_2O_5 films are then deposited by LPCVD at 400 or 450°C, using $Ta(OC_2H_5)_5$ and O_2 [1, 2]. Since Ta_2O_5 is known to chemically react with polysilicon, a reactively sputtered TiN layer is used [2].

Values of the maximum capacitance per unit area as high as 8.8 and 10.3 fF/μm^2 are observed for 15 and 10-nm-thick Ta_2O_5 layers on smooth polysilicon. These values correspond to dielectric constants of 14.9 and 11.6 if we neglect the interfacial nitride layer and assumed a full Ta_2O_5 thickness of 15 and 10 nm, respectively. If we assume that, in addition, a 2 nm thick nitride layer is grown during the RTN step, these values become 20.8 and 17.4, respectively. On rugged polysilicon, 15 and 10-nm-thick Ta_2O_5 films give capacitance values as high as 12.6 and 15.1 fF/μm^2. The devices I-V characteristics are shown in Fig. 2 for 15-nm-thick Ta_2O_5 layers. As can be seen, a strong stress polarity asymmetry is observed for the leakage current of smooth structures [6]. On the other hand, Fig. 2b shows a less asymmetry between positive and negative stress on rugged structures. These observations might indicate that the nitride thickness or quality is different on smooth and on rugged surfaces.

Fig. 3 illustrates the critical voltage (V_{crit}) required to induce 1 $\mu A/cm^2$ versus the capacitance per unit area of the different samples studied. For 3.3 V operated DRAMs, the critical voltage level of 1.65 V is also indicated in the figure. As can be seen, maximum capacitance values of 8.5 and 14 fF/μm^2 can satisfy these leakage requirements for smooth and rugged structures respectively. These values are considerably higher than the 6 fF/μm^2 that can be reached with ON films. Rugged structures present a capacitance improvement of about 65%, similar to that observed for ONO-based structures [5]. Fig. 3 also shows that (V_{crit}) decreases only slightly for films of higher capacitance on rugged electrodes while an abrupt decrease is seen on smooth samples. Rugged electrodes are, therefore, very attractive for Ta_2O_5 dielectrics and allow for further improvements on the maximum storage efficiency of these layers for future DRAM applications.

Fig. 4 presents time to 50% failure (T_{50}) values for smooth and rugged structures using a 15-nm-thick Ta_2O_5 film. Each point in the figure represents at least 30 measurements at a given stress level. In contrast to what was observed for ONO structures, Ta_2O_5 films on rugged structures exhibit larger lifetime values than on smooth structures at high stress voltage. The origin of this variation -- not yet fully understood -- is probably also linked to the difference in the effect of the RTN treatment mentioned above. For rugged structures, a linear extrapolation to $V_{cc}/2$ in Fig. 4 gives T_{50} values well above 50 years.

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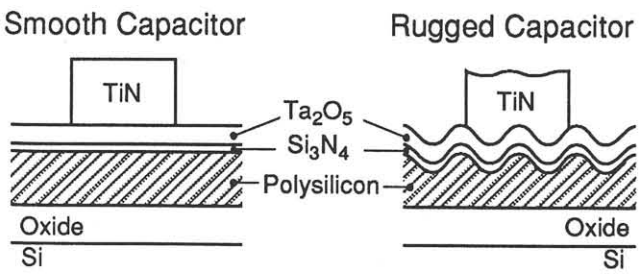

Fig. 1 Section of a smooth and rugged polysilicon/RTN/ Ta2O5/TiN capacitor.

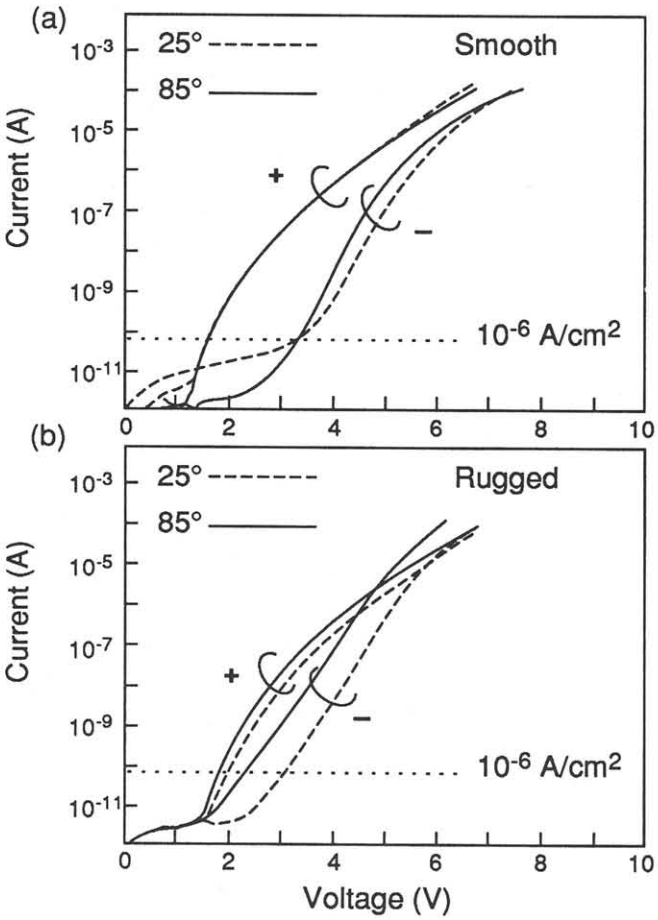

Fig. 2 I-V characteristics of (a) smooth and (b) rugged capacitor structures using a 15-nm-thick Ta_2O_5 dielectric film.

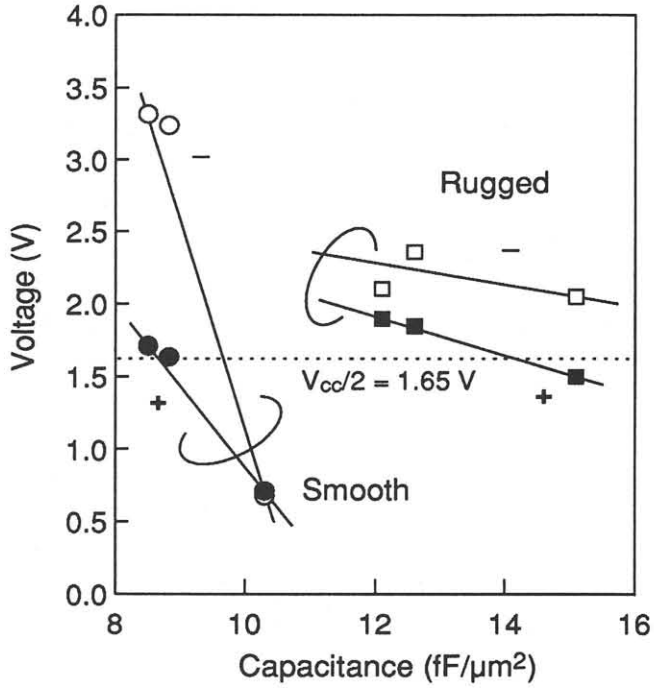

Fig. 3 Voltage required to induce a leakage of 1 μA/cm^2 versus capacitance per unit of capacitor projected area for the different samples investigated in this work.

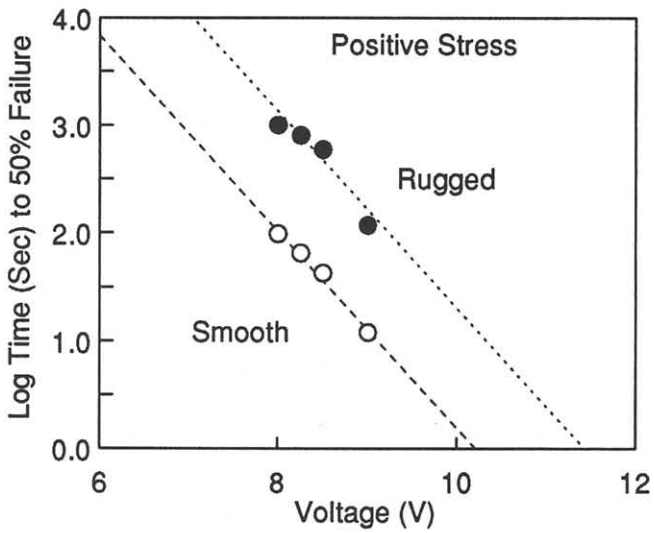

Fig. 4 Time to 50% failure versus stress voltage for the smooth and rugged capacitor structures of Fig. 2. All the points are measured with a positive bias applied on the top electrode (worst case condition).