The Effects of Polishing Damages and Oxygen Concentrations on Thin Gate Oxide Integrity (TOI)

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It has been reported that the TOI's are influenced by the surface microroughnesses and the densities of COP and FP (flow pattern) defects which increase with the increasing growth rate of CZ crystals. However, the reason why TOI's of FZ crystals and Epitaxial wafers are always perfect comparing to that of CZ crystals has not been clarified. The purpose of this paper is to show the mechamism of the degradation of TOI using the specimens with the different surface treatments and different oxygen concentrations.

The specimens with 4 levels of surface microroughness denoted as A, B, C and D including current prime device quality wafers C are intentionally produced by the variations of mechanical and chemical polishing components. Level A is the roughest, and is made efficiently using mechanical polishing commponents. The roughness of level B is in between A and C, and is prepared mainly by chemical factors. Level D is the smoothest surface prepared by balanced mainly using mechanical factors but also with small stock removal rate. The microroughnesses of specimens are measured by AFM below the area of $5 \times 5 \mu m^2$.

Two kinds of precleaning are used as described in the lower part of Fig. 1. The thin oxides of 100 A are grown by dry and wet methods. The voltage applied to the gate electrode is minus. When the breakdowns occur irreversibly within the current of 1 mA/cm², they are defined as "weak spot" defects.

The TOI's of CZ crystals are shown in Fig. 1. The level A wafers have high frequencies of the pin hole defects in all cases. On the other hand, the level B wafers show the almost perfect results which we have never seen in CZ crystals. Fig. 2 presents the RMS values depending on the mesured area on the 4 level surfaces. These values are directly measured on the device fabricated surfaces which polysilicon gates and oxides are stripped off. It can be said that the microroughnesses by AFM may correlate to their yields when the measurement area is smaller than $0.5 \times 0.5 \,\mu\text{m}^2$. The level B wafers have the lowest values of RMS. That is, from microscopic point of view, chemical polishing may produce smoother surfaces. On device yields, level C wafers of CZ crystals are superior than that of D wafers, although it is difficult to find the plausible explanation from the AFM results measured under $0.5 \times 0.5 \,\mu\text{m}^2$. On the other hand, FZ specimens doped with nitrogen (~2.5 $\times 10^{15}$ /cm³) obtain the ideal TOI independently of dry and wet oxidation and their microroughnesses as shown in Fig. 2.

In order to confirm that the above effects are caused by the out diffusing oxygen into the surfaces damaged by polishing, a series of TOI test adding MCZ crystal with intermediate oxygen concentration (~10ppma JEIDA) to CZ crystal (~19ppma) is prepared.

Three sets of specimens from the CZ and MCZ crystals are prepared; one is as polished, 2nd is chemically etched 0.5 μ m in depth with the mixtured solution of HF and HNO₃ and 3rd is etched 0.08 μ m in depth with NH₄OH / H₂O₂. As seen in Fig. 4, both oxygen concentrations and surface etching effects are clearly observed. The device yields of MCZ wafers are always superior than that of CZ wafers except polished-level A wafers. The TOI's of level A wafers are dramatically improved by the slightly etching. The best results of TOI's are given by the surfaces cleaned with NH₄OH / H₂O₂.

It may be concluded that during thin oxidation if the silicon surface is damaged by polishing, the oxide containing some defects which cause carrier traps is produced due to the out diffusing oxygen atoms. This interpretation is able to explain prausibly the reason why there is no actual relation between the TOI's using the as polished surfaces and the total yields of devices.

References

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