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Preoxide-Controlled Oxidation for Very Thin Gate Oxide

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Very thin gate oxide films with high insulating performance and high reliability are grown by controlling preoxide growth during the wafer heating up to thermal oxidation temperature using ultraclean oxidation method. The current level through the preoxide-controlled oxide is lower than that through the oxide including thicker preoxide, and the preoxide-controlled oxide has high reliability in term of hot electron injection.

1. INTRODUCTION

The electrical insulating performance and the reliability of very thin gate oxide films are crucial factors that determine the rate and the limitation of shrinking MOS ULSI devices. As the gate oxide becomes thinner, the influence of the Si surface microroughness and the native oxide on the integrity of the gate oxide can no longer be neglected. The existence of preoxide (= unintentionally grown initial oxide, i.e. native oxide and/or initial oxide grown during the wafer heating-up) in very thin gate oxide induces the degradation of the integrity, because the thickness ratio of the preoxide to net thermal oxide relatively increases as the gate oxide becomes thinner. Consequently, the integrity of the very thin oxide will be degraded and the scaling-down of MOS ULSI devices will be limited. It is, therefore, important to clarify factors determining the integrity of very thin oxide films in order to extend the limitation of gate oxide films.

In this paper, we describe the insulating performance and high reliability of very thin gate oxide films grown by controlling preoxide growth during the wafer heating up to thermal oxidation temperature using ultraclean oxidation method.

2. EXPERIMENTAL

The wafers used in this experiment were B-doped p-Si(100) Cz with the resistivity of 0.4-0.6 Ω·cm and P-doped n-Si(100) Cz with the resistivity of 8-12Ω·cm. Very thin oxide films were formed using the ultraclean oxidation system characterized by extremely low moisture and extremely low metal impurity concentrations in oxidation environment[1.2.3.4]. Ultraclean oxygen and argon gases were used as an oxidant and an inert gas, respectively. The moisture concentration in the argon gas was less than 5 ppb at the inlet of ultraclean oxidation system. Therefore, the thickness of the preoxide can be controlled in this ultraclean oxidation system, because the wafer is heated up to thermal oxidation temperature in ultraclean argon gas ambient.

The desorption of hydrogen from the HF cleaned Si surface is demonstrated to start at about 300°C and the Si surface consequently reacts with impurities (oxygen or moisture) at temperatures higher than 500°C[5]. So the HF cleaned wafers were heated up to 300°C in the ultraclean argon gas at the rate of 50°C/min, and then were intentionally oxidized at 300°C in the oxygen gas to form one molecular layer oxide as a passivation layer[6]. The wafer were again heated up to the thermal oxidation temperature of 900°C in the ultraclean argon gas to prevent preoxide growth.

3. RESULTS AND DISCUSSION

Figure 1 shows dielectric breakdown histograms of Al/SiO_2/n-Si(100) MOS diodes under the positively biased metal electrodes for 5.5nm oxides with(a) and without(b). The preoxide (0.4nm) was intentionally oxidized at 300°C in an ultraclean oxygen gas. The

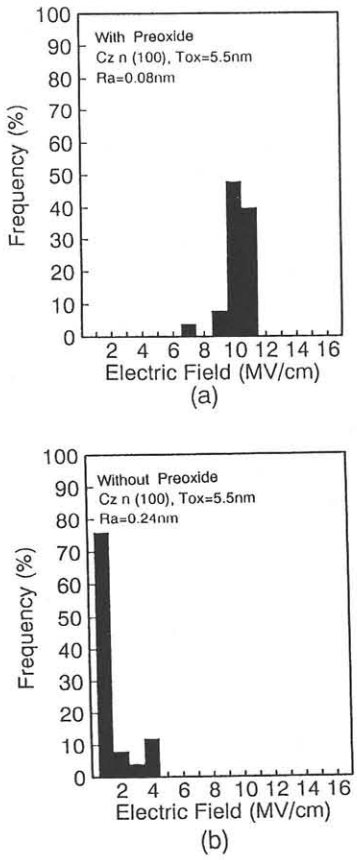

Fig.1 Dielectric breakdown histograms for $Al/SiO_2/n-Si(100)$ diodes with (a) without preoxide (b).

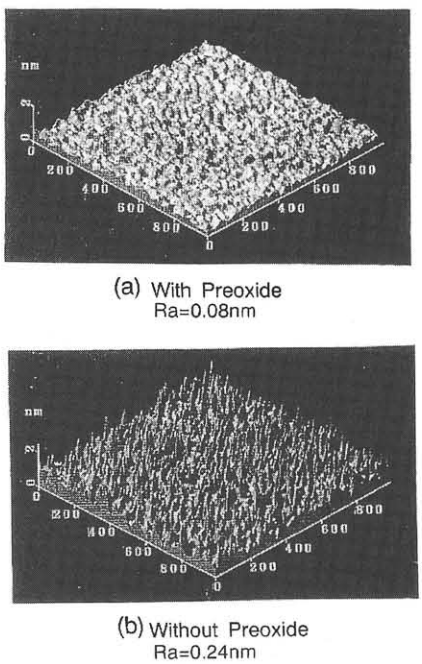

Fig.2 Atomic Force Microscope images of Si surface after Al and gate oxide removal of MOS diodes with (a) without preoxide (b).

wafer to form the oxide without preoxide was heated up to thermal oxidation temperature at 900°C in the ultraclean argon gas. Low field breakdown is little observed on (a), while low field breakdown events are observed on (b).

Figure 2 shows the Atomic Force Microscope images of Si surface after Al and gate oxide removal of MOS diodes shown in Fig. 1. A clear difference of the surface microroughness between (a) and (b) is observed. This result proves that the poor breakdown behavior on (b) is mainly caused by the increase of the interface microroughness. The increase of the surface microroughness is due to the etching of Si surface by trace oxygen or moisture in ultraclean argon gas during the heating-up process[6]. Therefore, the preoxide is helpful to form the very thin oxide with high reliability.

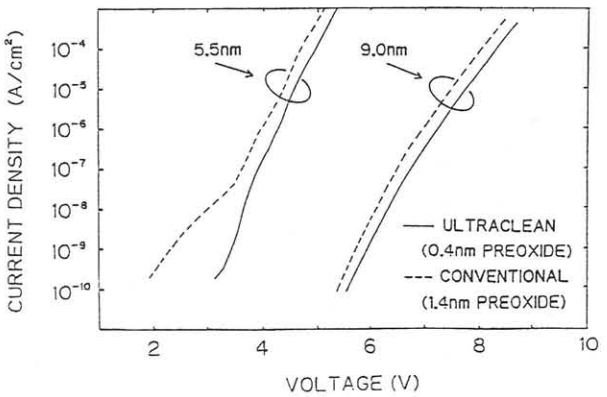

Fig. 3 Current density-voltage characteristics of n^+-poly-$Si/SiO_2/p-Si(100)$ diodes under negatively biased metal electrodes.

Figure 3 shows the current density-voltage characteristics of n^+-poly-$Si/SiO_2/p-Si(100)$ MOS diodes under the negatively biased metal electrodes for 5.5 nm and 9.0 nm oxides. The current level of ultraclean oxide with 0.4 nm preoxide is lower than that of conventional dry oxide with 1.4 nm preoxide over the range. For 5.5 nm oxide, the leakage current in the conventional dry oxide is much lager than that in the ultraclean oxide at the voltage lower than 3.5 V. These results indicates that the preoxide-controlled oxide has higher electrical insulating performance, particularly in the oxides having very thin thickness.

Figure 4 shows the threshold voltage shift of n-MOSFET as a function of the number of injected

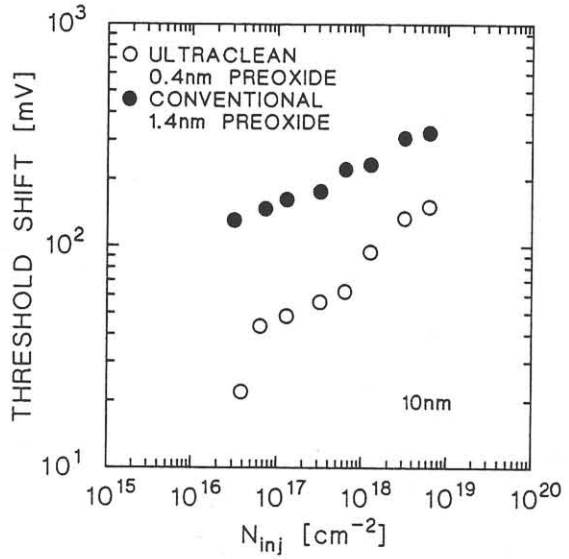

Fig. 4 Threshold voltage shift of n-MOSFET as a function of the number of injected electrons.

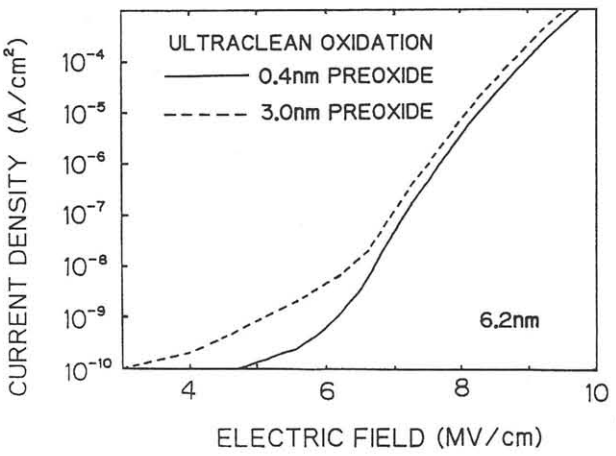

Fig. 5 Preoxide thickness dependence of current density-average electric field characteristics of n^+-poly-Si/SiO_2/p-Si(100) diodes.

electrons, where the gate oxide thickness of n-MOSFET is 10 nm. The threshold voltage shift for the ultraclean oxide with 0.4 nm preoxide is smaller than that for the conventional dry oxide with 1.4 nm preoxide. This means that the preoxide-controlled oxide has high reliability compared with the conventional dry oxide including thicker preoxide.

Figure 5 shows the effect of the preoxide thickness in ultraclean oxides on the current density-average electric field characteristics of n^+-poly-Si/SiO_2/p-Si(100) MOS diodes. The current level of the ultraclean oxide with 0.4 nm preoxide is lower than that of the ultraclean oxide with 3.0 nm preoxide over the range. The current level through the ultraclean oxide with 0.4 nm preoxide is not significantly increased, while the current through the ultraclean oxide with 3.0 nm preoxide is enhanced at low field region(≤6.5 MV/cm). This result proves that the presence of preoxide thicker than one molecular layer oxide in very thin gate oxide films induces the degradation of the electrical insulating performance.

4. CONCLUSIONS

We have demonstrated that the very thin ultraclean oxide formed by controlling the preoxide growth during the wafer heating up before thermal oxidation has high electrical insulating performance and high reliability. This work shows that preoxide control has strong potential in the formation of the very thin gate oxide with higher electrical insulating performance and reliability.

5. ACKNOWLEDGMENT

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6. REFERENCES

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