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A High Speed, Low Power P-Channel Flash EEPROM Using Silicon Rich Oxide as Tunneling Dielectric

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High speed and low power programming and low voltage erase are the desired features for the high performance flash EEPROM. In this paper, we demonstrate that by using **Silicon Rich Oxide (SRO)** as tunneling dielectric in **P-Channel EEPROM** cell, a high speed, low power and low voltage flash EEPROM can be accomplished. It is shown that the hot electron injection current in p-channel cell can be 2 orders of magnitude greater than in n-channel cell, while the channel current during programming in p-channel cell is 2 orders of magnitude less than in n-channel cell. A high speed programming, 1 μsec, can be achieved at low voltages, V_G = -3V and V_D = -5V. The erase can be accomplished at low voltage, V_G = 8V. This high speed, low power and low voltage cell can achieve 10^6 programming and erase cycles.

I. INTRODUCTION

In n-channel EEPROM or flash cells, channel hot electron injection into the floating gate from the channel has been used as the programming technique [1,2]. A high gate voltage is required in a n-channel cell during programming to enhance the injection efficiency of channel hot electrons and increase the programming speed. However, the use of high gate voltage during cell programming results in several drawbacks: (1) large power consumption due to high drain current and (2) charge loss in the programmed cell due to gate disturb. In this paper, we present a NEW FLASH EEPROM cell, the **P-channel FLASH EEPROM with SRO as tunneling dielectric**, which uses a different programming mode from a n-channel EEPROM. Programming at low gate voltage in the p-channel flash EEPROM allows high speed, low power, and high stability for the operation of the flash memory. By using SRO as tunneling dielectric, the low erase voltage can be achieved.

II. EXPERIMENTS

The processes used to fabricate the p-channel EEPROM cell are similar to the 0.25 μm technology reported in [3] except that the stacked poly gate process is added in fabricating EEPROM cell. The first polysilicon is implanted with 30 KeV, $6x10^{14}/cm^2$ phosphorus. A 15nm SRO followed by 7nm oxide deposited by Low Pressure Chemical Vapor Deposition (LPCVD) is formed on top of the first polysilicon. The second polysilicon which serves as the control gate is deposited and implanted with 45 KeV, $5x10^{15}/cm^2$ arsenic. The source and drain are implanted with 10 KeV, $3x10^{15}/cm^2$ boron. The n- and p-channel EEPROM cell without using SRO as interpoly dielectric are also fabricated on some of the wafers to be used for the comparison of programming currents.

III. RESULTS AND DISCUSSION

Programming of the p-channel EEPROM is accomplished by hot electron injection (generated by channel hot holes) into the floating gate. The hot electron injection efficiency in the p-channel EEPROM is maximized at low gate voltage since the oxide field at low gate and high drain voltages favors electron injection. Figure 1 illustrates the programming conditions of both n- and p-channel EEPROM cells and the corresponding energy band diagram near the drain during programming. Figure 2 shows the comparison of drain and gate currents of n- and p-channel cells. It clearly shows that the maximum hot electron current takes place at the low gate voltage in p-channel cell and at the high gate voltage in n-channel cell. Due to a larger assisting oxide field in the p-channel cell than in the n-channel cell during programming (as shown in Fig. 1), the electron injection efficiency (which is defined as the ratio of electrons collected at the floating gate to electrons generated in the channel) in the p-channel cell is more than 4 orders of magnitude greater than

in the n-channel cell, as shown in Fig. 3. In addition to high electron injection efficiency, Fig. 4 also shows that the p-channel cell has a much lower drain current than the n-channel cell at the maximum programming speed (maximum hot electron injection). The drain-to-gate current ratio (an indicator for power-delay product) of the p-channel cell is about 10^4x smaller than that of the n-channel cell, as can be derived from Fig. 4. These results suggest that a significant reduction of power consumption can be achieved by choosing a p-channel device for flash EEPROM cell.

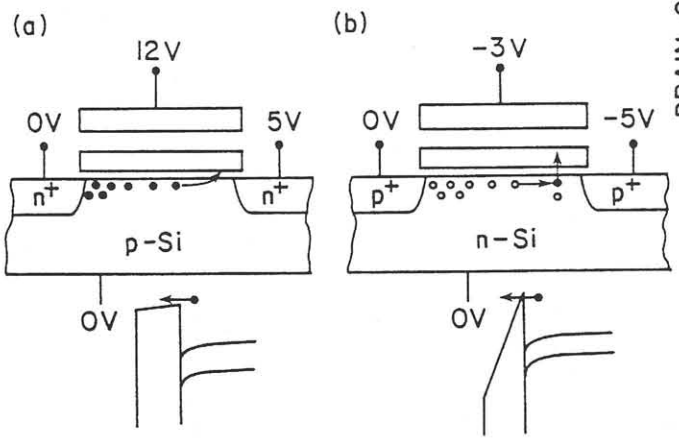

Fig. 1 Cross section and energy band diagram near the drain region of (a) n- and (b) p-channel EEPROM cells during programming

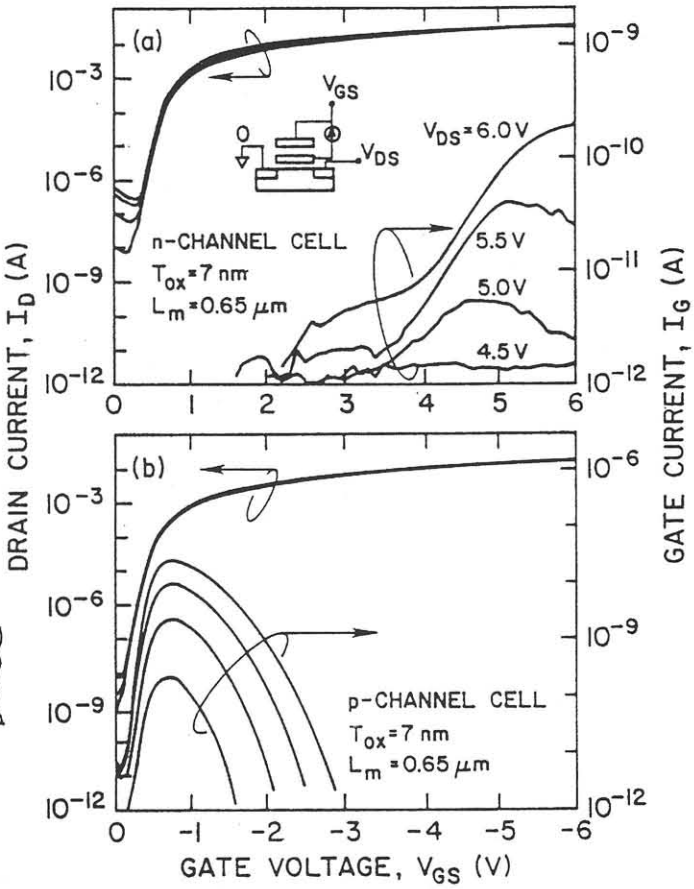

Fig. 2 Drain and gate current characteristics of (a) n- and (b) p-channel cells at various drain voltages.

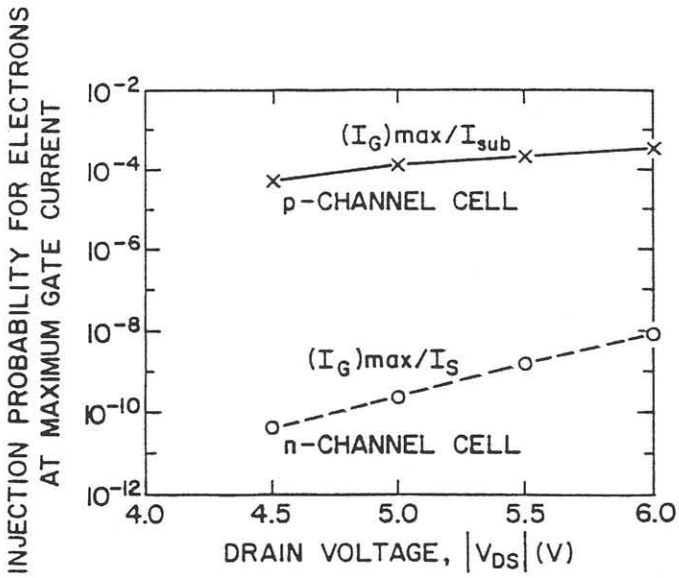

Fig. 3 Electron injection efficiency of p- and n-channel cells at maximum gate current condition.

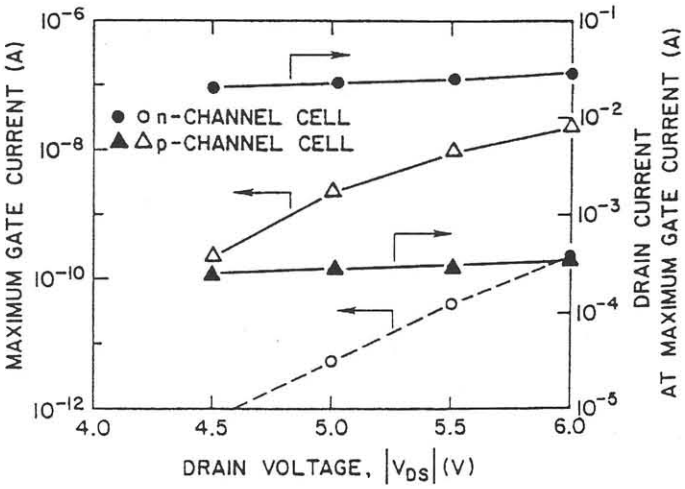

Fig. 4 Comparison of maximum gate current (related to speed) and drain current at maximum gate current (related to power) of p- and n-channel cells at various drain voltages.

The programming characteristics of stacked gate p-channel EEPROM cell is shown in Fig. 5. Due to the high hot electron injection current at low gate voltage, the cell can be programmed fast (1 μsec). By using Single Electron Injector Structure (SEIS) [4] which consists of a 7nm CVD oxide with a 15nm SRO underlayer as an interpoly dielectric, the erase is achieved by extracting electrons out of floating gate into the control gate. As shown in Fig. 6, the enhanced tunneling current is observed in the capacitor with SEIS by comparing with the capacitor without SEIS. The SEIS can achieve almost 2x field enhancement. Therefore, by using SRO as tunneling dielectric, the erase voltage can be greatly reduced. In our cell, the erase voltage is lowered down to 8V. The reliability of the p-channel cell is improved due to the fact that the gate oxide is not stressed at high field at either programming or erase condition. This cell can be programmed and erased up to 10^6 cycles (as shown in Fig. 7) before the program/erase window collapses.

IV. CONCLUSION

In summary, the p-channel EEPROM cell is shown to be a high speed, low power, and high stability cell due to high electron injection efficiency at low gate voltages. The power-delay product of the p-channel cell can be 10^4x smaller than that of the n-channel cell during programming. By using SEIS as interpoly tunneling dielectric, the erase voltage can be lowered and the reliability of the cell is improved. The p-channel EEPROM cell with SRO tunneling dielectric achieves 10^6 programming and erase cycles.

REFERENCES

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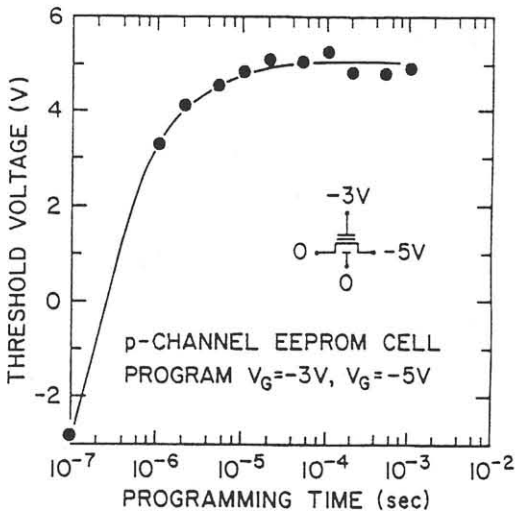

Fig. 5 Programming characteristics of p-channel EEPROM cell. L_{mask} = 0.8 μm

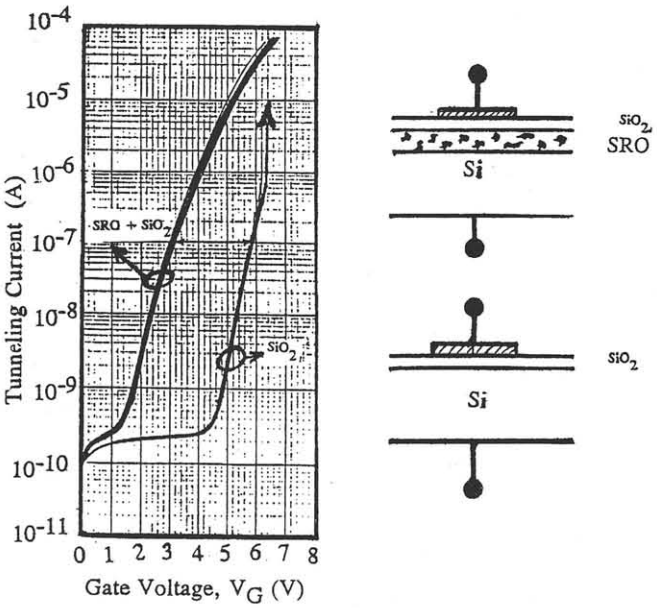

Fig. 6 Tunneling characteristics of SEIS film and deposited pure oxide.

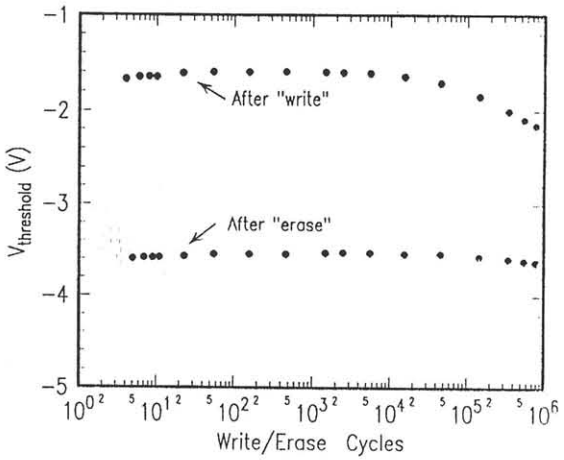

Fig. 7 Cycling characteristics of p-channel EEPROM cell.