Extended Abstracts of the 1992 International Conference on Solid State Devices and Materials, Tsukuba, 1992, pp. 155-157

Bias-Stress-Induced Stretched-Exponential Time Dependence of Charge Injection and Trapping in Amorphous Silicon Thin-Film Transistors

F.R. Libsch and J. Kanicki

IBM Research Division, Thomas J. Watson Research Center
P.O.Box 218, Yorktown Heights, New York 10598
Tel. (914) 681-5588 ; Fax. (914) 681-5576

We investigate the threshold voltage instabilities in nitride/oxide dual gate dielectric hydrogenated amorphous silicon (a-Si:H) thin-film transistors as a function of stress time, stress temperature and stress bias. The measured threshold voltage shifts are quantitatively modelled with a stretched-exponential stress time dependence where the stretched-exponent β cannot be related to the $\beta = T_{ST}/T_0$ but rather to $\beta \simeq T_{ST}/T_0^* - \beta_0$ for $T_{ST} \leq 80°C$; for $T_{ST} \geq 80°C$ the β is stress temperature independent. We have also found that β is stress gate bias independent. These findings are explained with a multiple trapping model with states located at the a-Si:H/a-SiN_x:H interface and in the a-SiN_x:H transitional layer close to the interface.

The mechanism responsible for the threshold voltage shift in nitride gate insulator transistors under time, temperature, and positive bias stress conditions is attributed in the literature to two possible degradation mechanisms: charge trapping in the gate insulator[1] and creation of dangling bond defects in the a-Si :H channel[2,3] near the a-SiN_x:H/a-Si:H interface. Because of this conflict there is a need to clarify some of the important questions concerning both these mechanisms before the final conclusions can be reached regarding the a-Si:H TFTs instability. The present paper is an attempt to provide some additional insight concerning the TFT's instability. The threshold voltage instabilities in nitride/oxide dual gate dielectric hydrogenated amorphous silicon (a-Si:H) thin-film transistors are investigated as a function of stress time, stress temperature and stress bias.

Figure 1 shows the evolution of a typical experimental transfer characteristics after positive gate bias stress of 30V for different stress times, which are indicated in the figure. This positive ΔV_t shift for positive stress gate bias is indicative of gate insulator charge trapping[4]. We have demonstrated in Figures 2 and 3 as a function of gate bias stress and temperature stress, respectively, that the threshold voltage shift, ΔV_t, in the transfer characteristics of all transistors in this in-

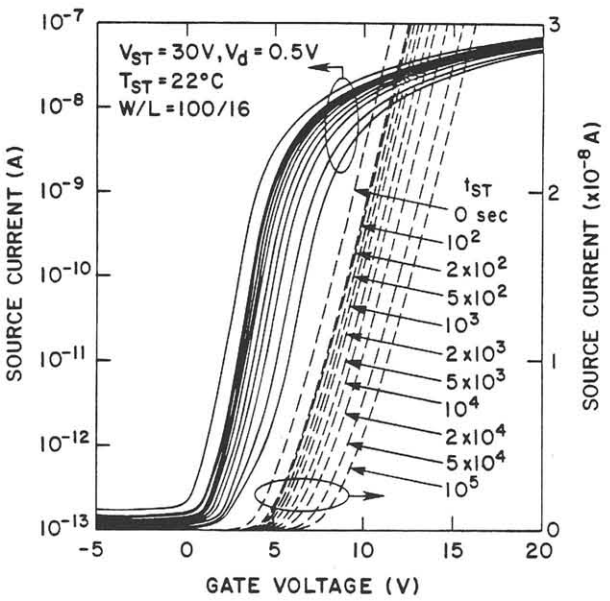

Figure 1: Effect of 30 V gate bias stress on the subthreshold (solid line) and linear region (dashed lines) transfer characteristics of an inverted-staggered a-Si:H thin film transitor incorporating a 50 nm N-rich nitride/200 nm oxide gate dielectric and a 60 nm thick a-Si:H layer with transistor dimensions of W/L = 100/16. In all cases the gate dielectric, the intrinsic a-Si:H channel and the P-doped S/D contact layers have been deposited at 250°C. During bias stress and measurement $V_d = 0.5V$ and $0.1V$, respectiveley. Note that the increasing stress times from 0 (unstressed) to 10^5 s shown in the figure produce a parallel shift of the transfer characteristics with an increase in the threshold voltage.

vestigation are well described by the stretched-exponential equation

$$|\Delta V_t| = |\Delta V_0| \left\{ 1 - \exp\left[-\left(\frac{t_{ST}}{\tau} \right)^{\beta} \right] \right\} \quad (1)$$

where $\Delta V_0 = V_g - V_{ti}$, is approximately the initial voltage drop across the insulator, $\tau = \tau_0 \exp(E_\tau / kT)$ is the characterisitic trapping time, where the thermal activation energy $E_a = E_\tau \beta$, with β being the stretched-exponetial exponent. In our model $E_\tau = E_a/\beta$ in Eq. (1) is the average effective energy barrier that carriers in the a-Si:H channel need to overcome before they can enter the insulator, with τ_0 being the thermal prefactor for emission over the barrier. For shorter stress times, smaller stress electrical fields, or lower stress temperatures, carriers hop or inject directly to lower-energy states; at longer stress times, larger stress electrical fields, or higher stress temperatures a larger fraction of states in the insulator near the interface will become filled, giving rise to an increasing probability of emision from these states. It is plausible that the amorphous structure of the gate insulator will lend itself to an appreciable number of band-tail states, which will act as transport states for the emitted lower-energy trapped state charge. This distibution of multiple traps yields a time dependence power law. Therefore, during the trapping there are many trapping events, and the motion between traps is nondispersive diffusive motion with a superimposed drift velocity, which is compatible with Eq. (1). We find that β and τ are stress bias independent while ΔV_0 demonstrates a noticeable dependence on gate bias stress. Our results in Figure 4 show that for $T_{ST} \leq 80°C$, $\beta \simeq (T_{ST}/T_0^*) - \beta_0$, where $T_0^* \simeq 229°K$ and $\beta_0 \simeq 1.04$, and for $T_{ST} \geq 80°C$, β becomes temperature independent with a β value of about 0.5. The obtained results are in contradiction with previously published data[2,5,6] that propose (i) $\Delta V_t \propto (V_{ST})^{\alpha} (\log t_{ST})^{\beta} \exp(-\Delta E/kT)$ with $\alpha \neq 1$, and $\beta \neq 1$, and (ii) $\beta = T_{st}/T_0$.

In summary, The obtained BTS induced threshold voltage shift data for stress temperatures from 22 to 125°C, stress biases from 25 to 65V, and stress times up to 10^5 seconds have been accurately modelled with a strectch-exponential time dependence with the power exponent independent of stress bias but dependent on stress temperature. The charge injection and trapping kinetics into the interface and the gate insulator is explain with a multiple trapping model.

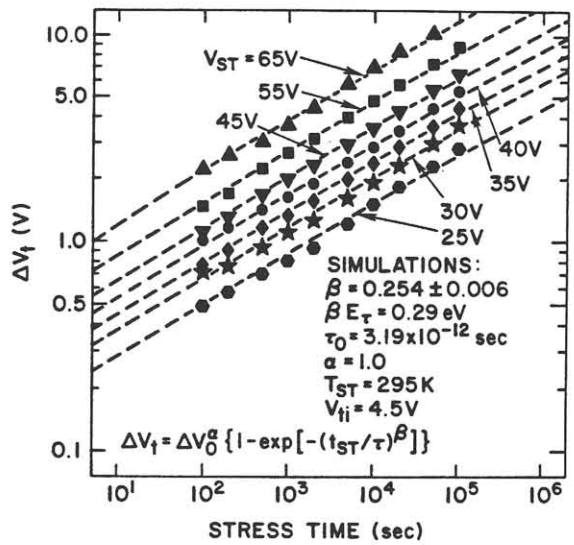

Figure 2: Threshold voltage shift, ΔV_t, vs stress time for gate bias stess voltages ranging from 25 to 65V and $T_{ST} = 22°C$. The symbols represent the data and the dashed lines the fits to Eq. (1) with the parameter values used listed in this figure.

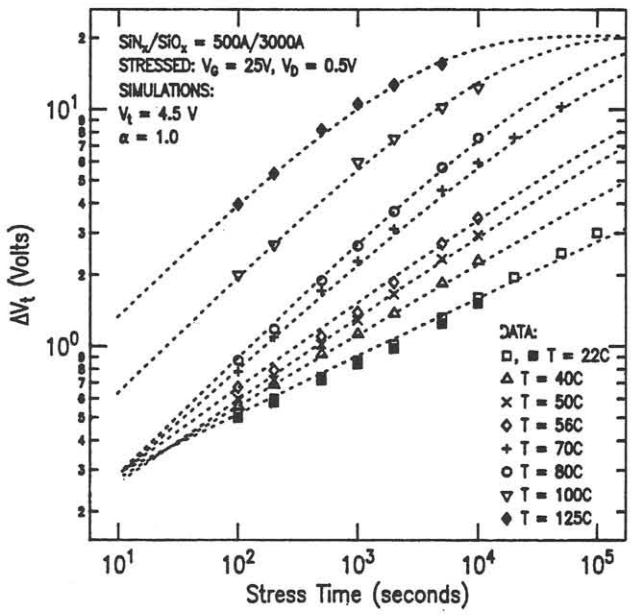

Figure 3: Threshold voltage shift, ΔV_t, vs stress time for different stress temperatures ranging from 22 to 125°C and for a positive gate bias of 25V. The symbols represent the data and the dashed lines the fit to Eq. (1) with the parameter values used listed in Figure 2.

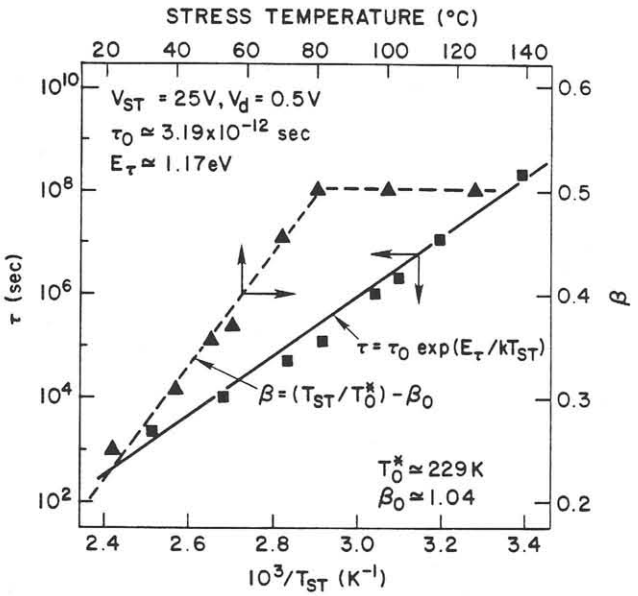

Figure 4: The variation of the extracted fitting parameters of τ and β as a function of stress temperature. The squares and triangles represent extracted values from the data of Figure 2, and the lines represent the bests fits to these data.

REFERENCES

1) A.V. Gelatos and J, Kanicki, Appl. Phys. Lett., 57(1990) 1197.
2) W.B. Jackson, J.M. Marshall, and M.D. Moyer, Phys. Rev. B, 39(1989) 1164.
3) M.J. Powell, C. van Berkel, A.R. Franklin, S.C. Deane, and W.I. Milne, Phys. Rev. B, 45(1992) 4160.
3) F.R. Libsch and J. Kanicki, Appl. Phys. Lett., to be published.
5) Y. Kaneko, A. Sassano, and T. Tsukada, J. Appl. Phys., 69(1991) 7301.
6) N. Ibaraki, M. Kigoshi, K. Fukuda, and J. Kobayashi, J. Non-Cryst. Solids, 115,(1989) 138.

ACKNOWLEDGEMENTS

The authors would like to thank the IBM Eastview Thin Film Transistor Processing Group for the devices used in this study. We are also grateful to Drs. R.R. Troutman and W.E. Howard for their review of this paper.