Extended Abstracts of the 1992 International Conference on Solid State Devices and Materials, Tsukuba, 1992, pp. 160-161

Impact of Low-Energy Ion-Implantation on Deep-Submicron Phosphorus-LDD nMOSFETs

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Low-energy ion-implantation has been required mainly for shallow source and drain formation of pMOSFETs with boron[1] . This is because boron, which is an only actual p-type dopant, has relatively long projected ranges of ion-implantation, and consequently forms deep junctions. NMOSFETs' shallow source and drain-junctions, on the other hand, can be easily formed with arsenic whose projected ranges are small and its thermal diffusivities are also small. Most reported deep-submicron nMOSFETs[2,3] , therefore, have adopted arsenic-source and drains so far. However, employing the low-diffusivity dopant, arsenic, only for nMOSFETs is not an advantage for CMOS-LSIs because the pMOSFETs' source and drain are formed with boron at the same time. In addition, the arsenic-source-drain nMOSFETs, even if the drain is LDD, show poor hot-carrier immunity because the diffusion-length is too small, and thus the drain(LDD) does not have a desirable graded profile to reduce an electric field when the thermal budget is optimized to pMOSFETs. On the other hand, the phosphorus-drain(LDD) generally shows a larger current drivability and a smaller substrate current than the arsenic-drain(LDD) formed with the same dose and projected range. Even if phosphorus is adopted to form shallow drain(LDD) for deep-submicron nMOSFETs using low-energy implantation, the problem still remains whether the thermal diffusion of the dopant is within a tolerant level.

This paper presents possibilities that the phosphorus-LDD will overcome the trade-off between the channel-shortening and the hot-carrier immunity by fabricating deep-submicron nMOSFETs with implantation at a minimum energy of 5keV and thermal treatments with the highest temperature of 850℃ after the implant. The channel regions were implanted with boron at 30keV to a dose of 6×10^{12}cm^{-2}, the gate oxide was 5nm thick, and the sidewall-spacers were formed by 100-nm thick CVD-oxide deposition and RIE. The heavily doped source and drain were formed by 20-keV, 4×10^{15}-cm^{-2}, arsenic implant. The threshold voltage dependence on channel length is shown in Figure 1. The lower the dose and the energy are, the smaller the short-channel effect is. The devices with 5×10^{12}-cm^{-2} LDD-implants do not show any rolloff of threshold voltage down to a 200-nm length. The lowering implant-energy still plays an important role in shallowing LDD in spite of the relatively high process temperature. I_D-V_{DS} characteristics of a transistor with a 150-nm long gate are shown in Figure 2. The LDD was formed by a 5-keV, 5×10^{12}-cm^{-2}, phosphorus implant and 40-nm long sidewall-spacers. This shortening sidewall-spacer length reduces parasitic resistances in the LDD. Figure 3 shows I_D -V_{GS} and I_{sub}-V_{GS} characteristics of the transistor. A relatively high drain current of I_D/W=0.57mA•μm^{-1} at V_{DS}=V_{GS}=2V is obtained without silicidation. The substrate current of I_{sub}/W=48nA•μm^{-1} at V_{DS}=2V is low enough to avoid the hot-carrier degradation.

The channel doping was done by conventional 30-keV, 3×10^{12}-cm^{-2} boron implant before gate-oxidation, hence, the slope of the impurity concentration depth profile is not steep. The uniform doping profile has been considered as vulnerable to the short-channel effect. The experimental results suggest that the making source-drain shallow may still be more important and practical to realize high-performance deep-submicron devices than a "vertical doping engineering[2,4,5] " proposed by several institutions.

In conclusion, the low-energy implantation is very effective to suppress the short-channel effect of the phosphorus-LDD configurations. The phosphorus-LDD nMOSFETs show good performance even in a deep-submicron regime, and they are suitable for thermal budget adjustment to pMOSFETs.

References

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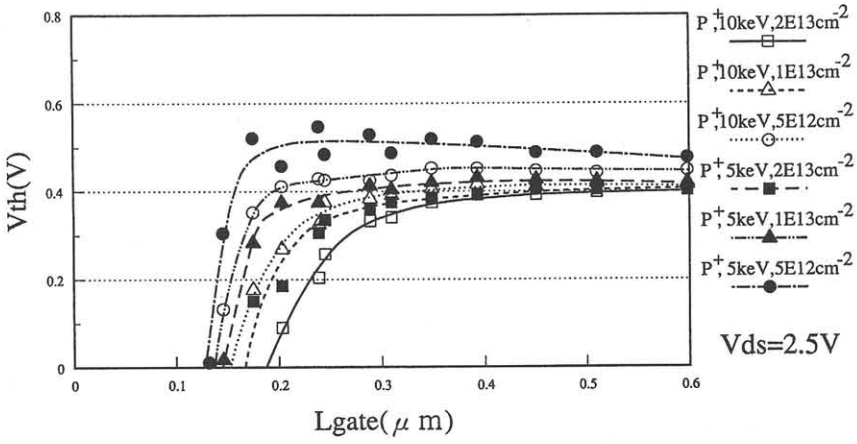

Figure 1. Dependence of threshold voltage on gate length for various LDD-implant conditions. W=5μm, t_{ox}=5nm, the sidewall-spacers are 100nm long, and the channel doping dose is $6\times10^{12}cm^{-2}$.

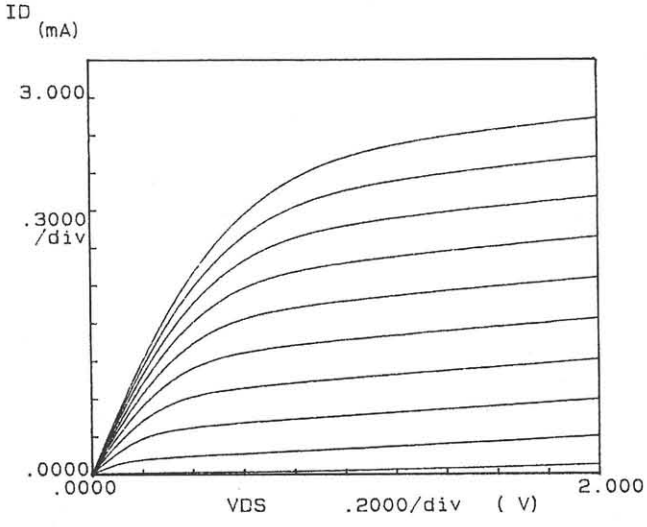

Figure 2. I_D -V_{DS} characteristics of a transistor with a 150-nm long gate. The sidewall-spacer is 40nm long. W=5μm, t_{ox}=5nm, and the channel doping dose is $3\times10^{12}cm^{-2}$.

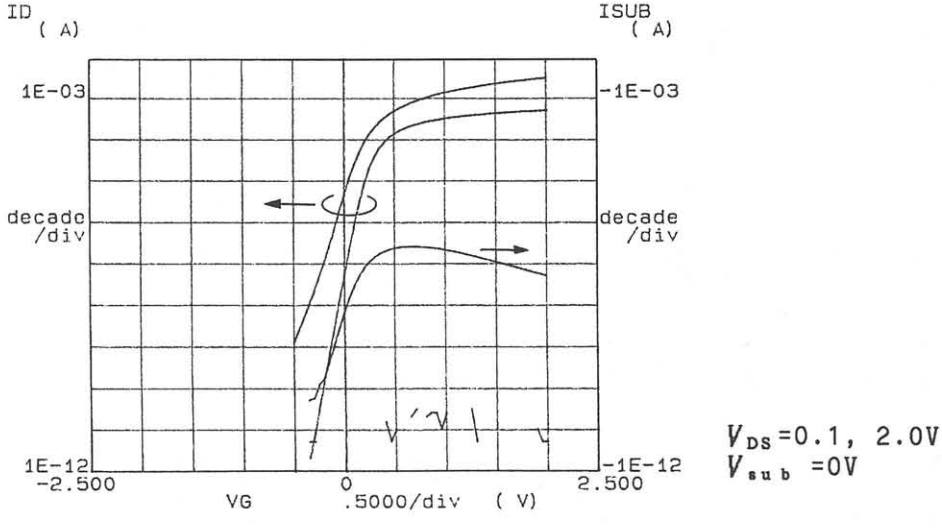

Figure 3. I_D and I_{sub} -V_{GS} characteristics of a transistor with a 150-nm long gate (the same transistor as shown in Figure 2).