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Silicon Nitride Film for High-Mobility Thin-Film Transistor by Hybrid-Excitation Chemical Vapor Deposition

Shigeichi YAMAMOTO^{*} and Masatoshi MIGITAKA Toyota Technological Institute, 2-12-1, Hisakata, Tempaku, Nagoya 468, JAPAN phone 052-802-1111, Fax. 052-802-6069

Hybrid-excitation by plasma and light chemical vapor deposition (CVD) has been investigated to make silicon nitride (SiN_x) films for the gate insulator of thin-film transistors (TFTs). A low-defect density SiN_x /silicon (Si) interface has been developed and high field-effect mobility (μ_{FE}) TFTs are expected to be used in large-area and high-resolution displays.

The purpose of this study is to deposit SiN_x film on Si with low-defect density interface at a substrate temperature below 300 °C. The coplanar-type TFTs using the SiN_x gate-insulators were fabricated by hybrid-excitation CVD.

It is difficult to get an excellent SiN_x/Si interface by plasma-enhanced CVD because of ion-bombardment damage. Although photo-enhanced CVD is expected to form an excellent interface, reported effective trapped-carrier density (N_{eff}) at $SiN_x/(100)Si$ is generally above 1 x 10^{11} cm⁻². We estimate that this is due to the shortage of nitrogen-source (e.g. ammonia, NH₃) photoproducts in the early stage of photo-CVD.

To overcome this problem, we developed a hybrid-excitation CVD technique (Fig. 1). In the deposition, the product of NH_3 gas which was previously decomposed by plasma was irradiated by 184.9-nm and 253.7-nm UV-rays with disilane (Si₂H₆) gas. The N_{eff} at SiN_x/(100)Si interface could be reduced below 2 x 10¹⁰ cm⁻². To further improve the interface, this technique added a direct-nitrification treatment at the silicon surface using NH_3 gas before the film deposition. As a result of this treatment the N_{eff} was reduced by half.

A typical coplanar-type TFT was fabricated by the following steps. First, an amorphous silicon (a-Si:H) film was deposited by plasma-enhanced CVD on an insulating substrate at 280 °C. Secondly, source and drain electrodes were formed by photo-lithography with evaporated aluminum (Al) on the a-Si:H film. The bared a-Si:H surface was treated and a 50-nm-thick SiN_x film gate-insulator was deposited at 280 °C as described in the above technique. A gate electrode was formed with evaporated Al. Post annealing were not carried out.

Figure 2 shows the effect of direct-nitrification treatment time on the $\mu_{\rm FE}$ of the TFT whose a-Si:H film thickness is 100-nm. The TFT fabricated without treating the a-Si:H surface shows a relatively high value of $\mu_{\rm FE}$ (1.7 cm²/(Vs)). The value of $\mu_{\rm FE}$ is further improved by the treatment and reaches a maximum (4.6 cm²/(Vs)) at 7.5 min. Figure 3 shows an effect of a-Si:H film thickness on the $\mu_{\rm FE}$ of the TFT whose a-Si:H surface was treated for 7.5 min. A TFT with high $\mu_{\rm FE}$ (5.3 cm²/(Vs)) is successfully fabricated at an a-Si:H film thickness of 156-nm, as shown in Fig. 3. The TFT showed threshold voltage of 4.1 V and an on/off current ratio exceeding 10⁶.

* On leave from New Materials Research Laboratory, TOAGOSEI Chemical Industry Co., Ltd.



Fig. 1. Cross-sectional view of hybrid-excitation system.



a-Si:H surface direct-nitrification time (min)

Fig. 2. Field-effect mobility of a-Si:H TFT as a function of direct-nitrification treatment time of the a-Si:H surface.



Fig. 3. Field-effect mobility of a-Si:H TFT as a function of a-Si:H film thickness.