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Subthreshold Slope in Ultra Thin-Film SOI MOSFET's and Its Two-Dimensional Analytical Modeling down to 0.1 μm Gate Length

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As the trend towards ULSI and 0.1μm MOSFET structures requires low voltage operation and hence low threshold voltages, it is increasingly important to study the subthreshold slope factor and to give physical insight into its parameter dependence. This paper analyses the S-factor in ultra thin-film fully depleted SOI MOSFET's and its degradation at short gate length, thereby presenting for the first time a two-dimensional analytical model. Based on an approach in [1], it is unlike formerly reported models (e.g.[2]) able to describe the S-factor in miniaturized devices down to 0.1μm gate length. Three degradation mechanisms were clarified: parasitic channel edge capacitances, modulation of the current inversion channel width and back channel conduction.

Fig. 1 shows the S-factor variation with SOI thickness in dependence on the channel doping. In contrast to the common expectation of a degraded slope for higher doping shown at the right hand side (PD) of the figure, it is found as a unique feature of fully depleted SOI MOSFET's that the S-factor can be improved by increasing N_A. Although this phenomenon is also present in large devices as long as t_{SOI} is thin enough to ensure full depletion, the improvement is essential for small dimensions as shown in the left part. Therefore, it is useful towards 0.1μm regime where the structure requirements to ensure device operation are t_{ox}, t_{SOI} and t_{BOX} to be 5, 20 and 50nm, respectively [3]. In order to clarify these effects and hence be able to utilize them for device design, an analytical model has been developed. Assuming a parabolic vertical potential distribution across the channel, the 2D-Poisson equation is solved and expressions for the slope factor are derived, as shown in Fig. 2.

In the model it is considered that an increasing surface electric field reduces the weak inversion channel width of subthreshold diffusion current. This results in a correction term which predicts the S-factor improvement for higher channel doping where the relative change of the field is smaller. Fig. 3 illustrates the rise of parasitic capacitances C_{SE} and C_{DE} at source and drain ends of a short channel device due to the fact that in these regions electric force lines bend outward in the buried oxide and terminate at the bottom of source and drain [4]. The analytically derived potential variation with gate voltage represents the common capacitor network like in the long channel case and an additional channel length dependent term which can be attributed to C_{DE} and C_{SE}. The model predicts that the S-factor degradation can be reduced by further decreasing t_{SOI} and t_{ox} or lowering the S/D doping.

In the low doped short channel ($L<0.15$ μm) devices subthreshold current flow occurs at the back channel/oxide interface. This strongly degrades the S-factor and is accounted for by a factor which describes the coupling between front and back surface potentials. Fig. 4 shows that the S-factor dependence on gate length predicted by the analytical model is in good agreement with results of numerical simulation. The strong short channel degradation at lower doping is the result of the above mentioned three effects whereas at higher doping only the parasitic channel edge capacitances have to be considered.

[1] K. K. Young, IEEE ED-36, 399 (1989)
[2] D. J. Wouters et al, IEEE ED-37, 2022 (1990)
[3] H. O. Joachim et al, IEICE SDM 91-201, 51 (1992)
[4] M. Yoshimi et al, IEEE ED-36, 493 (1989)

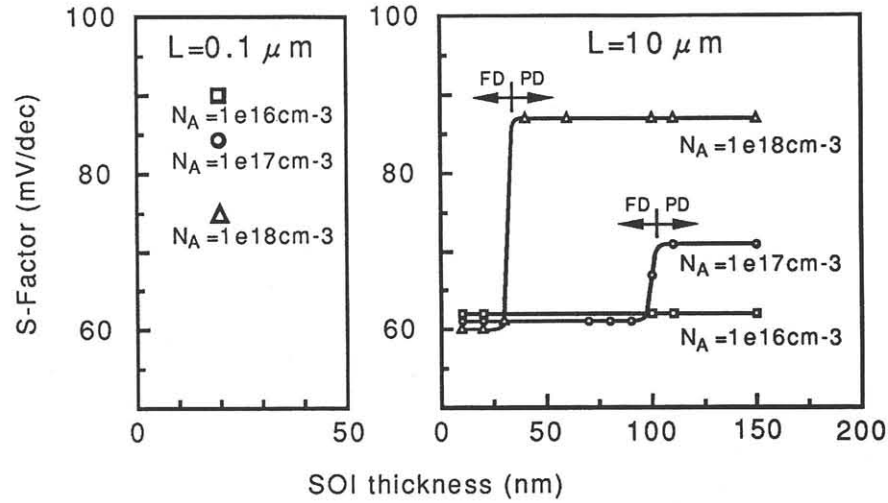

Fig. 1
Numerically simulated S-factor for different channel dopings in partially (PD) and fully depleted (FD) SOI MOSFET's with L=10 μm and in a scaled down FD device structure with L=0.1 μm

$$\frac{1}{S} = \frac{1}{\ln 10} \cdot \left(\frac{q}{kT} - \underbrace{\frac{1}{E_{SF}} \cdot \frac{\partial E_{SF}}{\partial \Psi_{SF}}}_{\text{correction term due to modulation of weak inversion channel width}} \right) \cdot \frac{\partial \Psi_{SF}}{\partial V_G}$$

$$\frac{\partial \Psi_{SF}}{\partial V_G} = \frac{1 + CAP}{CAP} \cdot \left\{ 1 - \underbrace{\frac{\sinh g/2}{\sinh g} \cdot \left(\sqrt{\frac{T_{DE}}{T_{SE}}} + \sqrt{\frac{T_{SE}}{T_{DE}}} \right)}_{\text{parasitic channel edge capacitance term}} \right\}$$

$$g = \sqrt{a} \cdot L \qquad CAP = \frac{C_{OX}}{C_{SOI}} + \frac{C_{OX}}{C_{BOX}}$$

$$T_{SE} = \frac{b}{a} + \varphi_{BI} - \left(\frac{b}{a} + \varphi_{BI} + V_D \right) \cdot e^{-g}$$

$$T_{DE} = \frac{b}{a} + \varphi_{BI} + V_D - \left(\frac{b}{a} + \varphi_{BI} \right) \cdot e^{-g}$$

$$a = \frac{2(1 + CAP)}{t_{SOI}^2 \cdot \left(1 + \frac{2C_{SOI}}{C_{BOX}} \right)}$$

$$b = \frac{q \cdot N_A}{\varepsilon_{Si}} - \frac{2CAP}{t_{SOI}^2 \cdot \left(1 + \frac{2C_{SOI}}{C_{BOX}} \right)} \cdot V_G - \frac{2}{t_{SOI}^2 \cdot \left(1 + \frac{2C_{SOI}}{C_{BOX}} \right)} \cdot V_{SUB}$$

Fig. 2
Model equations for the case of front channel conduction
(E_{SF} front surface electric field,
Ψ_{SF} front surface potential,
φ_{BI} built-in potential)

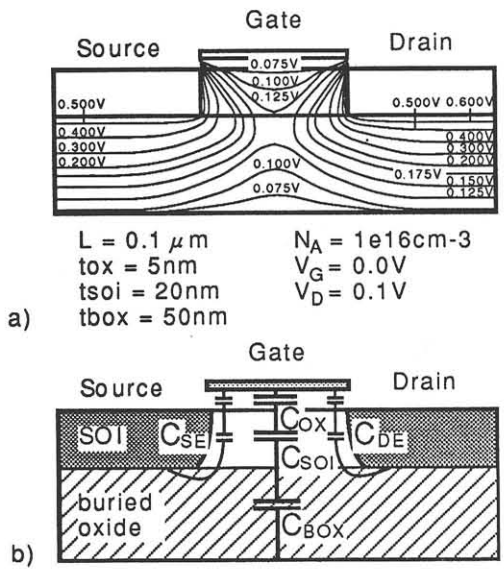

Fig. 3
a) Simulated potential distribution of a 0.1 μm SOI MOSFET in subthreshold region
b) Capacitance model (C_{SE} , C_{DE} are the channel edge capacitances)

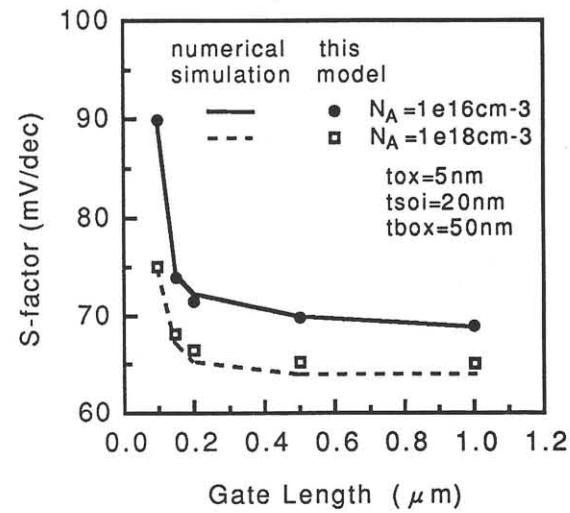

Fig. 4
Comparison of the analytical model with results of numerical simulation