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An Analytical Model for Substrate and Gate Current of Stressed SC-PMOSFET in the Saturation Region

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In this paper, we present the change of the lateral electric field distribution with the trapped electron charge and the analytical models for I_{sub} and I_g of stressed SC-PMOSFET in the saturation region. To derive the hot electron induced electric field in the damage region, Ko's box model was modified. Our modified field model can explain the reduction of the lateral electric field with the trapped charge and the decrease of I_{sub} and I_g of stressed SC-PMOSFET. Calculated I_{sub} and I_g of stressed SC-PMOSFET using our modified lateral electric field agreed with experimental data.

I. INTRODUCTION

Hot-electron-induced MOSFET degradation imposes limits on VLSI scaling. Physical mechanism for hot electron damage has been extensively studied in NMOSFET and BC-PMOSFET [1-2]. There has been a growing interest in surface-channel PMOSFET with p^+ polysilicon gates for deep-submicron CMOS technology due to its advantage in regard to the short channel effect compared with the BC-PMOSFET. Recently, physical degradation mechanism and several analytical models for substrate current (I_{sub}) and gate current (I_g) models of SC-PMOSFET have been studied [3-4]. However, those models have been derived from the impact ionization process for the fresh device and have ignored the change of the lateral electric field distribution by the electron trapping near the drain region. Also, previous models can not explain the I_{sub} and the I_g of stressed devices and logarithmic time dependence of those currents.

In this paper, we will first present the change of the lateral electric field distribution for the electron trapping and the analytical models for I_{sub} and I_g of stressed SC-PMOSFET in the saturation region. We also explain the logarithmic time dependence of I_{sub} and I_g from the extension of our models. The test devices used in this study were conventional SC-PMOSFET with t_{ox}=150Å, W/L_{eff}=20/0.8 μm, and x_j=0.38μm.

II. The MODEL

1. Lateral electric field

In order to get an exact model for I_{sub} and I_g of stressed SC-PMOSFET in the saturation region, Ko's box model in the saturation region was modified like Fig. 1 which illustrate the analysis of the velocity saturation region under the condition of electron trapping in the oxide. To derive the hot electron induced lateral electric field, Gauss's law was applied to the rectangular box.

$$-E_{sat}\, x_j + E(y)\, x_j + \frac{\varepsilon_{ox}}{\varepsilon_{si}}\int_0^y E_{ox}(0,k)dk + \frac{1}{\varepsilon_{si}}\int_0^y qN_t dk = \frac{qN_d}{\varepsilon_{si}} x_j\, y + \frac{qN_m}{\varepsilon_{si}} x_j\, y \quad (1)$$

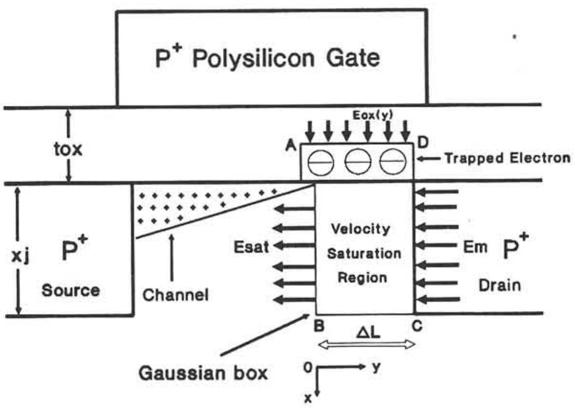

Fig. 1 Schematic digram of stressed SC-PMOSFET.

where E_{sat} is channel field at which the carriers reach saturation velocity, $E_{ox}(y)$ is vertical electic field at the surface without trapped electron, qN_d is donor density within the Gaussian box, qN_m is mobile charge density, and qN_T is trapped electron charge in the gate oxide.

In writing this equation, we have made three approximations. First, hot electrons from impact ionization were trapped in the oxide layer near drain region. Second, the distribution of trapped electron is uniform. Third, the length of trapped electron in the damage region is longer than that of the pinch-off region. From the above eq. (1), we have the following the lateral electric field and potential distribution in the y-direction.

$$E(y)=E_{sat}\cosh\left(\frac{y}{l}\right)-\frac{qN_t}{lC_{ox}}\sinh\left(\frac{y}{l}\right) \tag{2}$$

$$V(y)=V_{dsat}+lE_{sat}\sinh\left(\frac{y}{l}\right)-\frac{qN_t}{C_{ox}}\cosh\left(\frac{y}{l}\right)+\frac{qN_t}{C_{ox}} \tag{3}$$

The maximum lateral electric field(E_m) at the drain end of the channel is $E(y=\Delta L)$.

$$E_m=E(y=\Delta L)=E_{sat}\cosh\left(\frac{\Delta L}{l}\right)-\frac{qN_t}{C_{ox}}\sinh\left(\frac{\Delta L}{l}\right) \tag{4}$$

$$V_d=V_{dsat}+lE_{sat}\sinh\left(\frac{\Delta L}{l}\right)-\frac{qN_t}{C_{ox}}\cosh\left(\frac{\Delta L}{l}\right)+\frac{qN_t}{C_{ox}} \tag{5}$$

Equations (4) and (5) can be combined to yield

$$\Delta L=l\cdot\ln\left[\frac{lE_m+V_d-V_{dsat}-qN_t/C_{ox}}{lE_{sat}-qN_t/C_{ox}}\right] \tag{6}$$

$$E_m=\left[\frac{(V_d-V_{dsat}-qN_t/C_{ox})^2}{l^2}+E^2_{sat}-\left(\frac{qN_t}{lC_{ox}}\right)^2\right]^{1/2} \tag{7}$$

2. An analytical models for Isub and Ig

I_{sub} and I_g in SC-PMOSFET result from electron generation by impact ionization induced by the channel holes as they travel from the source to the drain. Since the impact ionization rate is a strong function of channel electric field, I_{sub} and I_g strongly depend on the lateral electric field. We used the reported I_{sub} and I_g model of [4]. However, our models are different from eqs.(8) and (9) in that E_m is a function of trapped electron charge.

$$I_{sub}\simeq\frac{A_i}{B_i}\,lE_mI_d\exp\left(\frac{-B_i}{E_m}\right) \tag{8}$$

$$I_g\simeq 0.5\,\frac{I_{sub}\,t_{ox}}{\lambda_r}\left(\frac{\lambda E_m}{\phi_b}\right)^2 P(E_{ox})\exp\left(\frac{-\phi_b}{E_m\lambda}\right) \tag{9}$$

III. RESULTS AND DISCUSSION

Figures 2 and 3 show the lateral electric field distribution with channel position within the damage region. We assumed that N_t has a Gaussian distributed function $N_o\cdot\exp[-0.5(y-y_o)^2/\sigma^2]$ in Fig. 2, and compared the difference of electric field distribution in the damaged region with the uniformly distributed N_t in Fig. 3. Here N_o, σ, and y_o with respect to the drain junction are 1.0×10^{12} cm^{-2}, 0.15 μm, and $0.1\mu m$, respectively. Figure 4 shows the dependence of trapped electron charge(N_t) on the lateral electric field with the drain voltage. It can be seen that there is a decrease in field with the increase in the trapped electron charge. The reduction in field reduces the energy of the carriers, and results in less charge being injected into the oxide. This results are similar to Doyle's numerical simulation results [5]. In Fig. 5, the calculated hot-electron damage region length(ΔL) increases with N_t and this results in the increase of drain current of stressed SC-PMOSFET in the saturation region. Figures 6 and 7 show that I_{sub} and I_g of stressed SC-PMOSFET decreases with stress time (or N_t) due to the decreased lateral electric field, respectively. When the N_t is zero, the shape of I_{sub} and I_g are the same as those of the fresh devices and those results are very similar to the other's results [4]. From Figs. 6 and 7, I_{sub} and I_g of stressed device after stress time of 1000 sec are reduced due to the reduced lateral electric field which decrease the injection of the electron into the oxide. The reasonable agreement between the measurement data and calculated values with $N_t=8.1\times10^{11}$ cm^{-2} demonstrates the validity of our lateral electric field model with the trapped electron charge.

IV. CONCLUSION

A new approach for analytical models of I_{sub} and I_g of stressed SC-PMOSFET in the saturation region is presented. This model includes the change of the maximum lateral electric field distribution by the electron trapping near the drain region. Good agreement has been obtained between the modeled and experimental data. The extension of our models can be extremely useful in explaining the logarithmic time dependence of I_{sub} and I_g for stressed SC-PMOSFET.

REFERENCES

[1] C. Hu, et al., IEEE Trans. Electon Devices, ED-32(1985)375.
[2] F. Matsuoka, et al., IEEE Trans. Electon Devices, ED-37(1990) 1487.
[3] Y. Tang, et al., IEEE Electon Device Lett. EDL-11(1990) 203.
[4] T. Ong, et al., IEEE Trans. Electon Devices, ED-37(1990) 1658.
[5] B. Doyle, et al., IEEE Trans. Electon Devices, ED-37(1990) 1301.

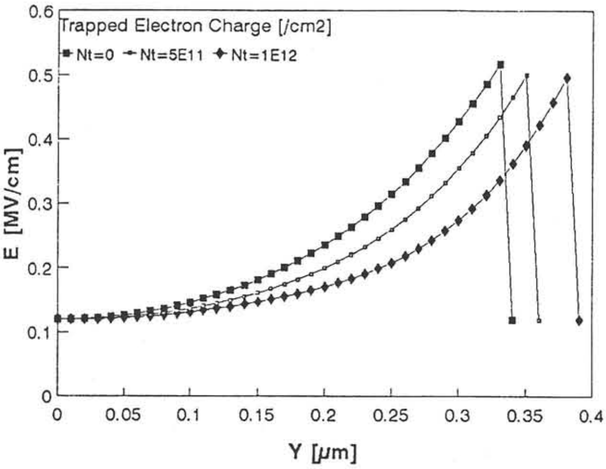

Fig. 2 Lateral electric field distribution with channel position within the damage region.

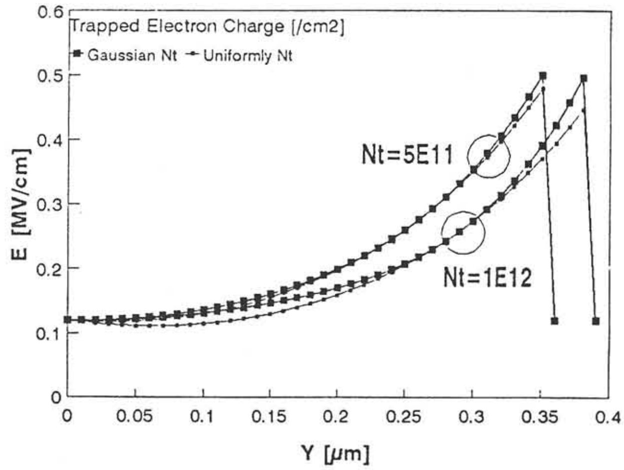

Fig. 3 Lateral electric field distribution with channel position for N_t=Gaussian and N_t=Uniformly damage profile.

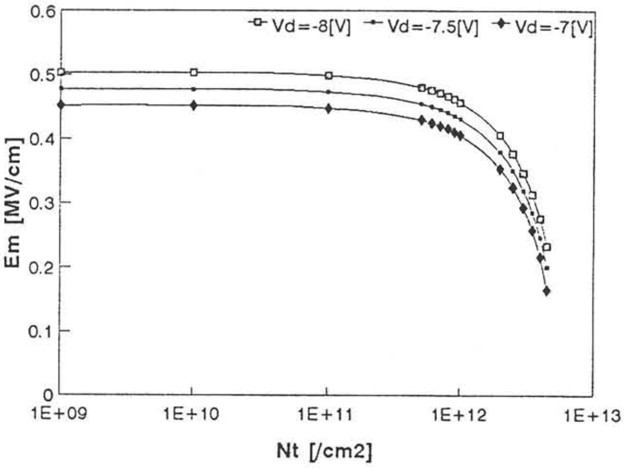

Fig. 4 Correlation between maximum lateral electric field and the trapped electron charge.

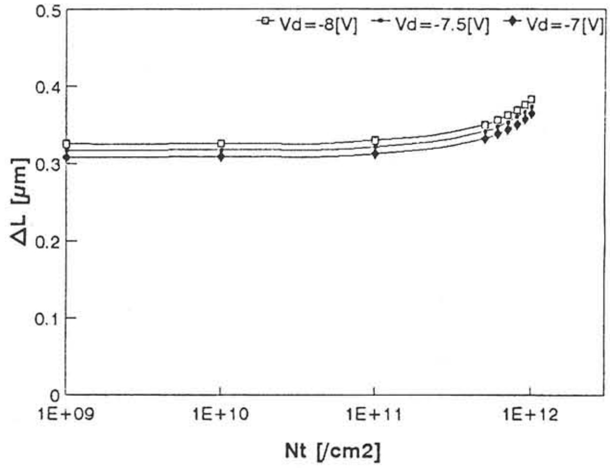

Fig. 5 Correlation between the hot-electron damage region length(ΔL) with the trapped electron charge.

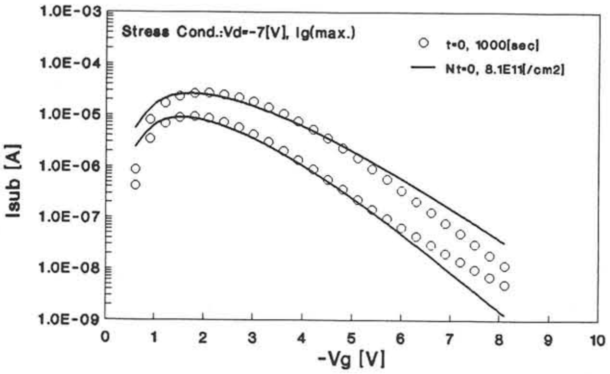

Fig. 6 Isub of fresh(t=0 or N_t=0) and stressed (1000 sec or $N_t=8.1 \times 10^{11}$ cm^{-2}) SC-PMOSFET.

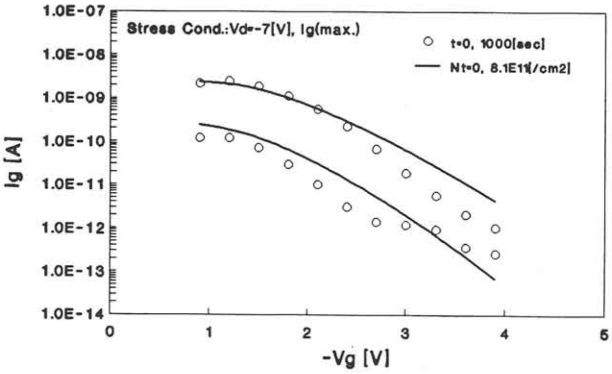

Fig. 7 Ig of fresh(t=0 or N_t=0) and stressed (1000 sec or $N_t=8.1 \times 10^{11}$ cm^{-2}) SC-PMOSFET.