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Determination of the Interface Trap Density in MOSFETs from the Subthreshold Slope Measurement

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Interface trap densities at SiO_2/Si interfaces of MOS transistors(MOSFETs) are extracted by measuring subthreshold slope dependence on substrate bias. This method enables a direct characterization of SiO_2/Si interfaces for small size MOSFETs. The application of this technique to a large size MOSFET shows a good agreement with the result obtained from the high-frequency/quasi-static capacitance-voltage(C-V) technique for a MOS capacitor. Futhermore, substrate dopant concentration can also be extracted from the subthreshold slope measurement and shows a good agreement with the result obtained from the body-effect measurement.

I. Introduction

Subthreshold region is particularly important for low-voltage, low-power applications, such as when MOSFETs are used as a switch for digital logic and memory applications, because the subthreshold region describes how the switch turns on and off.[1,2] Therefore, the factors determining subthreshold slope, such as gate oxide thickness, channel dopant concentration, and interface trap density, should be optimized enough to satisfy a required on-off current ratio.

One of the most important parameters for the estimation of the MOS device reliability is the interface trap density, D_{it}. To the present, D_{it}s are evaluated by using large MOS capacitors.[2,3] For VLSI MOSFETs, it is difficult to extract D_{it} by using the conductance method, the high-frequency/quasi-static capacitance-voltage(C-V) method, or the deep level transient spectroscopy(DLTS), due to their small capacitor areas. The subthreshold slope technique was developed for MOSFETs, but it is not applicable to small size MOSFETs, and only the average interface trap density could be obtained at the surface potential near 1.5 times of the Fermi potential.[4]

In this paper, a simple method to obtain D_{it} in the range of the surface potential between midgap and threshold, directly from the subthreshold slope measurement of a MOSFET, is suggested. D_{it}s for various size MOSFETs were extracted from the subthreshold measurement and compared with those for large capacitors from the high-frequency/quasi-static C-V measurement. Substrate dopant concentration can also be extracted from the subthreshold slope measurement. D_{it}s after gate-bias(high field) stress on a MOSFET were also extracted. Considering channel doping profile, substrate bias range, and short channel effect, limit of this method was discussed.

II. Equations for extracting the interface trap density

In depletion region, where the surface potential, ψ_s, is larger than the Fermi potential, ϕ_F, and smaller than $2\phi_F$, ψ_s can be approximated as[2,3]

$$\psi_s = (V_G - V_{FB}) - (a^2/2\beta)\{[1+ 4(\beta V_G - \beta V_{FB} - 1)/a^2]^{1/2} - 1\}, \quad (1)$$

where V_G is the gate voltage, V_{FB} is the flat-band voltage, β is defined as q/kT, and a is defined as $\sqrt{2(\varepsilon_s t_{ox}/\varepsilon_{ox} L_D)}$ where L_D is the extrinsic Debye length. The subthreshold slope $S(\equiv dV_G/d\log(I_{DS}))$ is given by[3]

$$S \approx (kT/q) \ln 10 \cdot [1 + (C_D + C_{it})/C_{ox}], \quad (2)$$

where C_D is the differential capacitance of the semiconductor depletion layer and

$$C_{it} = qD_{it}. \quad (3)$$

Other notations have their usual meanings. Equations (1) and (2) are adequate forms for MOSFETs with low interface trap density or thin gate oxide. C_D is approximated as $[q\varepsilon_s N_A/2(\psi_s + |V_{BS}| - 1/\beta)]^{1/2}$ in weak inversion region, where V_{BS} is the substrate bias.

As V_{BS} approaches the infinity, S approaches S_∞ which has the value of

$$S_\infty \approx (kT/q) \cdot \ln 10 \cdot (1+C_{it}/C_{ox}) \quad (4)$$

and the slope L_s of S vs. $(\psi_s + |V_{BS}| - 1/\beta)^{-1/2}$ is $(kT/q)\ln 10 \cdot (q\varepsilon_s N_A/2)^{1/2}(t_{ox}/\varepsilon_{ox})$. Therefore, the substrate dopant concentration, N_A, can also be extracted from L_s. L_s may be lowered for short channel MOSFET due to the charge sharing between gate and source/drain.[5] To avoid this lowering, the application of this method has to be restricted to the channel length showing the negligible reduction of

threshold voltage. When substrate biases are applied to the substrate, ψ_s could be estimated by the assumption that equal drain currents at various V_{BS}'s have the identical surface potential.

III. Experimental and Results

MOSFETs in this experiment were fabricated by using a conventioal polysilicon gate CMOS process. At first, V_{FB}s have to be extracted from MOSFETs to calculate surface potentials. The threshold voltage, V_T, is related with the flat-band voltage as[3]

$$V_T = V_{FB} + 2\phi_F + \sqrt{[2q\varepsilon_s N_A(2\phi_F + |V_{BS}|)]}/C_{ox} \quad (5)$$

and the threshold voltage shift, ΔV_T, becomes

$$\Delta V_T = \gamma [\sqrt{(2\phi_F + |V_{BS}|)} - \sqrt{(2\phi_F)}] , \quad (6)$$

where the body-effect parameter, γ, is defined as $\sqrt{(2\varepsilon_s qN_A)}/C_{ox}$. If we measure threshold voltages of large size MOSFET as a function of substrate bias, substrate dopant concentration can be estimated by using eq. (6). Then, subtracting $2\phi_F$ from the value of the intersection point of the extrapolated line to the V_T axis results in V_{FB}.

If N_A is roughly known, ϕ_F can be estimated with the relative accuracy. Measuring the V_T dependence on V_{BS} and inserting ϕ_F obtained from the first estimation into eq. (6), we can determine N_A more accurately than the roughly known value for the first stage. If we perform this process once more, N_A and ϕ_F could be evaluated very accurately.

Figure 1 shows the body effect of n-MOSFET with the gate oxide of 100 Å and W/L of 30 μm/30 μm. The measured γ is about 0.497 $V^{3/2}$ so that the calculated substrate dopant concentration is about 8.8×10^{16} cm^{-3} and V_{FB} is about -0.8 V.

An example of the extraction of D_{it}s for various surface potentials in the n-MOSFET(Fig. 1) is shown in Fig. 2. All three L_s's are nearly equal to 0.015 $V^{3/2}$ and correspond to the dopant concentraion of 9.4×10^{16} cm^{-3}, which is nearly the same as the result from the body-effect measurement. S_o (≡ (kT/q) ln 10) is about 58.5 mV/decade at room temperature. The measured S_∞ is 60.36 mV/decade for the surface potential of 0.536 V so that the calculated D_{it} by eq. (3) is 6.8×10^{10} $eV^{-1}cm^{-2}$.

Figure 3 shows the energy distribution of interface traps in the band gap for a n-MOSFET from the subthreshold slope measurement and that for a capacitor from the high-frequency/quasi-static C-V method. In n-MOSFET, only interface traps in the upper half of the band gap are detectable by the subthreshold slope measurement. D_{it} of the MOSFET is somewhat larger than that of the capacitor. As ψ_s approaches $2\phi_F$ toward the conduction band, D_{it} increases exponentially, showing a similar result to that obtained from the high-frequency/ quasi-static C-V measurement.

Another example is shown in Fig. 4, where a MOSFET was gate-bias stressed at V_G of 19.6 V. S_∞ becomes larger with increasing stress time, due to the increase of interface trap charge. ψ_s was selected to be 1.5 ϕ_F. The measured S_∞ is 73.3 mV/decade for the stress time of 180 s so that the calculated D_{it} by eq. (3) is 2.65×10^{11} $eV^{-1}cm^{-2}$.

Figure 5 shows the energy distribution of interface traps in the band gap for the MOSFET(Fig. 3) from the subthreshold slope measurement before and after the gate-bias stress. After the 20 V stress for 90 s, the average interface trap density in the gap was increased as much as about 2×10^{11} $eV^{-1}cm^{-2}$ compared with the original one.

IV. Discussions

As forementioned, our method for the extraction of interface trap density is very useful for small size (short-channel) MOSFETs. However, the drain-induced-barrier-lowering(DIBL) induces the increase of surface potential, which restricts the application of this method to short-channel MOSFETs. In this analysis, the channel dopant concentration was assumed to be constant, while usual MOSFETs have non-uniform ones due to the channel ion-implantation. Step profile is commonly used to model threshold voltage or body effect constant. If the depletion layer edge exists within the step profile, the average dopant concentration of the step profile may be considered to be N_A. However, if the depletion layer edge exceeds the step profile, N_A may not definetely be determined so that the linearity of L_s becomes worse. The application of this method to MOSFETs with nonuniformly doped channel is also limited by this fact.

In addition, the surface mobility dependence on effective surface electric field and the effective inversion layer thickness dependence on substrate bias were neglected in this analysis. However, the subthreshold current depends mainly on surface potential, while the surface mobility and the effective channel thickness are minor factors contributing to the subthreshold current compared with the surface potential. This was confirmed by the fact that the slopes, L_ss, are nearly equal, independent of surface potential.

V. Conclusion

Interface trap densities at SiO_2/Si interfaces of MOSFETs were extracted by measuring the subthreshold slope dependence on substrate bias. This method enables the analysis of SiO_2/Si interfaces for small size MOSFETs. Required parameters for extracting the interface density, such as surface dopant concentration, the Fermi potential, and flat-band voltage, were not extracted from a MOS capacitor but from a MOSFET. The application of this technique to a large size MOSFET showed a good agreement with the result obtained from the high-frequency/quasi-static C-V technique for a MOS capacitor. Futhermore, substrate dopant concentration can also be extracted from the subthreshold slope measurement and showed a good agreement with the result from the body-effect measurement. Therefore, the gate oxide quality, passing through full precessing steps or TDDB/

hot carrier stresses, can easily be monitored, in which degradations may be confined to the oxide near the polysilicon edge.

Acknowledgement
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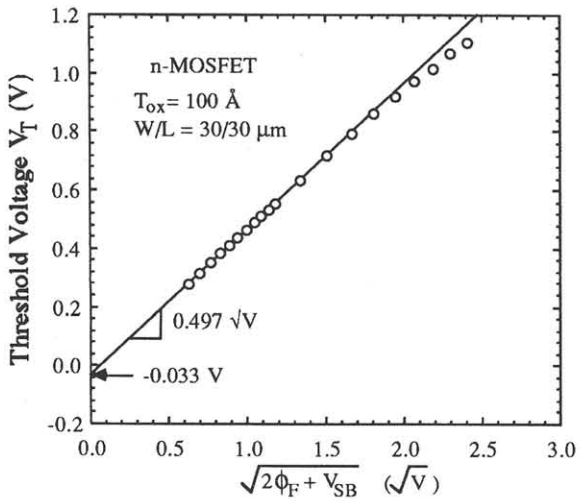

Fig. 1. Body-effect of an n-MOSFET.

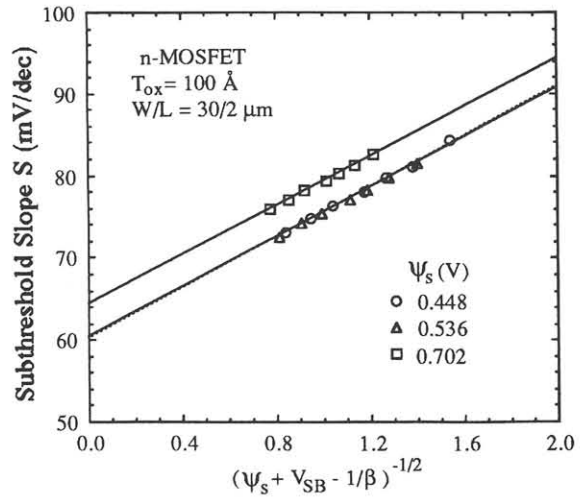

Fig. 2. The subthreshold slope dependence on the substrate bias with surface potential as a parameter.

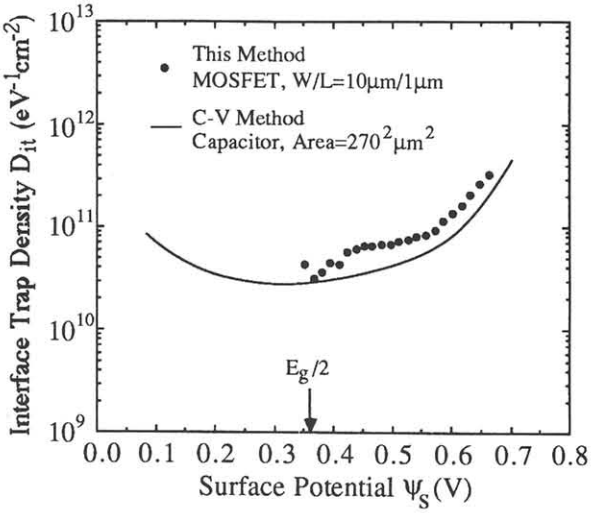

Fig. 3. The energy distribution of interface traps in the band gap for n-MOSFET from the subthreshold slope measurement (•) and that for a capacitor from the C-V method (-).

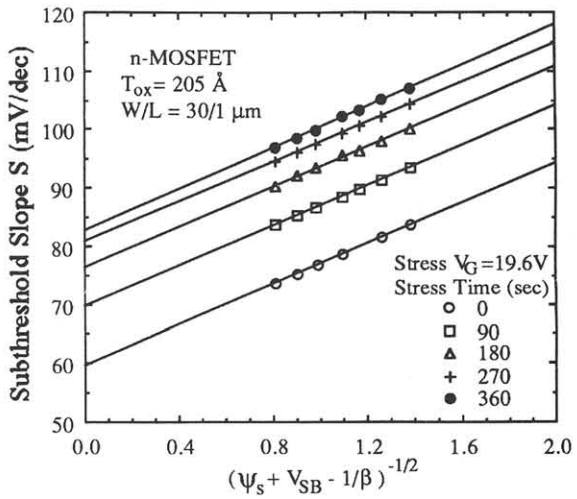

Fig. 4. Increase of the subthreshold slope by the high gate-bias stress, with stress time as a parameter.

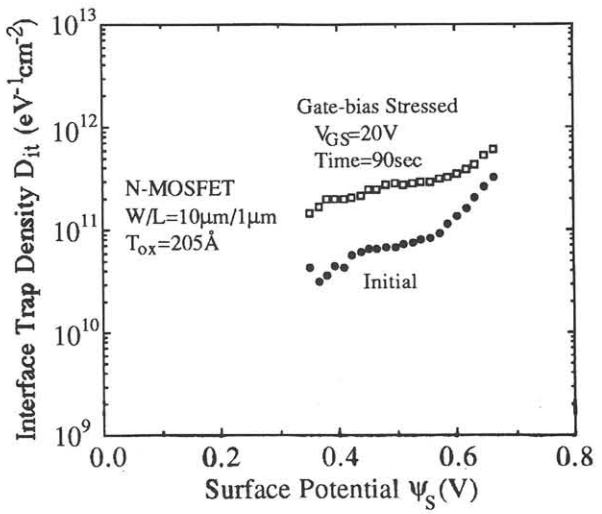

Fig. 5. The energy distribution of interface traps in the band gap for the initial n-MOSFET (•) and the gate-bias stressed MOSFET (□).