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Channel Hot-Carrier Programming in EEPROM Devices

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ABSTRACT

A novel programming method for FLOTOX EEPROM device is presented and investigated. The device is equivalent to an EPROM device in parallel with an EEPROM structure. With an extra negative source and substrate voltage, both channel hot-electron injection under the gate oxide of the EPROM structure and F-N tunneling under the tunnel oxide of the EEPROM structure are enhanced at programming. Moreover, the enhanced erased threshold voltages are observed under this negative source and substrate voltage. With the proper control of this biasing scheme, the select transistor in the EEPROM cell can be eliminated and the cell area can be reduced efficiently.

1. INTRODUCTION

In the operation of the EEPROM devices, a high voltage around 14V is applied to the control gate or the drain to program or erase the cell through F-N tunneling, respectively. Erasing using a negative voltage is also proposed for a better endurance[1]. Generally, the higher programming/erasing voltage causes difficulties in circuit design, reliability, and operation compatibility with digital ICs, etc.. In this work, a new programming/erasing scheme is proposed to explore the possibility of reducing the programming voltage. In the proposed scheme, the inherent parasitic EPROM device in the FLOTOX EEPROM structure is used to generate hot carriers for programming and enhance tunneling for erasing.

2. PROCESS TECHNOLOGY AND CELL STRUCTURE

The FLOTOX EEPROM cell under investigation was fabricated by 1.8μm n-well, double level polysilicon and double metal, CMOS process. The thickness of the tunnel oxide, the gate oxide, and the inter-poly oxide is 10nm, 35nm, 55nm, respectively.

The main process and device parameters of the fabricated EEPROM device are listed in Table I.

Fig.1 shows the cross-sectional view of the FLOTOX EEPROM cell which has a tunnel area 1.96μm2 and an effective channel length 1.8μm. As may be realized from the device cross-sectional view, the EEPROM cell structure can be represented by an EEPROM device in parallel with an EPROM device, both connected to a switching device (MOSFET) as shown in Fig.2. The EPROM device, formed by the gate oxide together with source and drain, is seldom programmed in the conventional programming operation of the EEPROM device.

Table I Main Process and Device Parameters of the Measured FLOTOX EEPROM Devices

P-SUBSTRATE RESISTIVITY	45-65 Ω-cm
TUNNEL OXIDE THICKNESS	100A
GATE OXIDE THICKNESS	350A
FLOATING GATE THICKNESS	4000A
CONTROL GATE THICKNESS	4500A
INTERPOLY OXIDE THICKNESS	550A
SOURCE/DRAIN N+ IMPLANT	1.0E22 cm-3
CELL SIZE	88um2
CHANNEL LENGTH	1.8um
TUNNEL OXIDE AREA	1.96um2

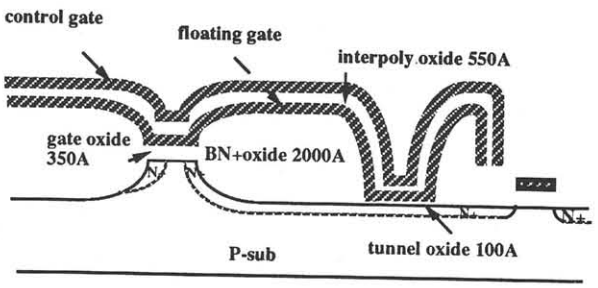


Fig.1 The cross-sectional view of the FLOTOX EEPROM cell.

3. PROGRAM AND ERASE CHARACTERISTICS

The proposed biasing scheme of the EEPROM is shown in Fig.3 where a negative voltage is applied to source and substrate and the drain is grounded. The programming is done by applying a positive gate voltage whereas the erasing is done by a negative gate voltage. The oxide capacitance's among gate, source, and drain[2] are shown in Fig.4.

Fig.5 shows the programmed/erased threshold voltages as a function of substrate and source voltage with different control-gate voltage amplitudes from 16V to 12V. It is seen that the threshold voltage magnitude after programming or erasing increases with the increase of the negative substrate and source voltage. The phenomena can be explained as follows. In the programming with a high positive gate voltage, the negative substrate and source voltage simultaneously increases the channel electrons and the lateral electric field along the channel. This enhances the hot-electron generation and the generated hot electrons inject through the gate oxide into the floating gate. Thus the threshold voltage after programming increases. On the other hand, the negative substrate and source voltage in the erasing case increases the negative voltage on the floating gate through the coupling capacitance's as shown in Fig.4. This increases the electric field across the tunnel oxide and enhances the F-N tunneling . Thus the threshold voltage becomes more negative after erasing.

3.1. PROGRAM

The comparisons of the threshold voltage after programming with and without the negative substrate and source voltage are shown in Fig.6(a). With Vs=Vsub=-5V, the written threshold voltage increase is about 2V. Even with a low gate voltage of 10V in programming which causes no F-N tunneling, the hot-electron injection still causes a 2V threshold shift. But with a lower gate voltage below 10V, the shift is lower at the fixed bias -5V.

3.2. ERASE

Fig.6(b) shows the comparisons of the erased threshold voltage with and without the negative source and substrate voltage. At the same gate voltage, the erased threshold voltage increases in magnitude of 0.5V with Vs=Vsub=-5V.

From the above results, it can be seen that a negative voltage applied to the source and substrate could reduce the programming and erasing gate voltage in magnitude while keeping the same programmed and erased threshold voltage, respectively. The biasing conditions for the cell to achieve the programmed threshold voltage Vtw=5V and the erased threshold voltage Vte=0V are listed in Table II.

Keeping the erased threshold voltage a little larger than 0V, the current flow resulted from the depleted-

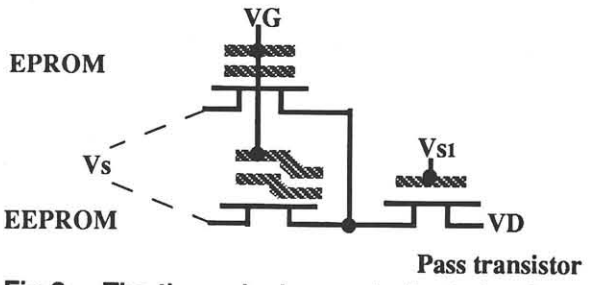
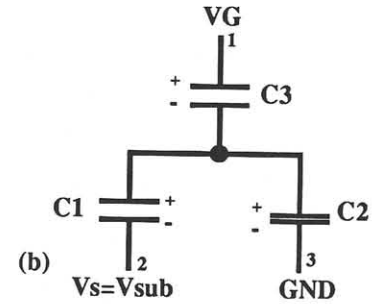


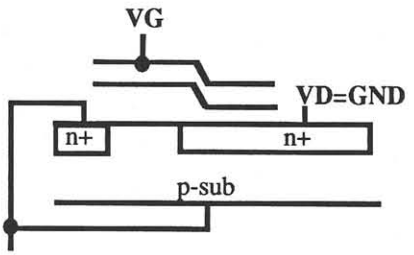
Fig.2 The three-device equivalent circuit.



C1 : Gate oxide capacitor
C2 : Tunnel oxide capacitor
C3 : Interpoly oxide capacitor

Node1: control gate
Node2: substrate
Node3: drain under tunnel oxide

Fig.3 The biasing scheme of the EEPROM device.



Vs=Vsub=negative voltage

Fig.4 The equivalent circuit for the oxide capacitances in the EEPROM device.

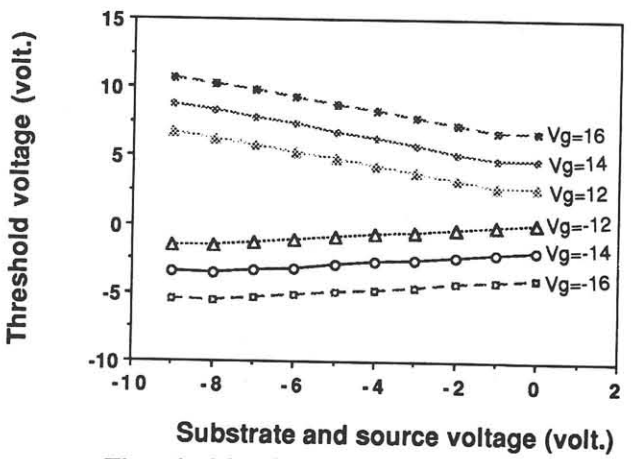


Fig.5 Threshold voltage as a function of Vs=Vsub with different gate voltages.

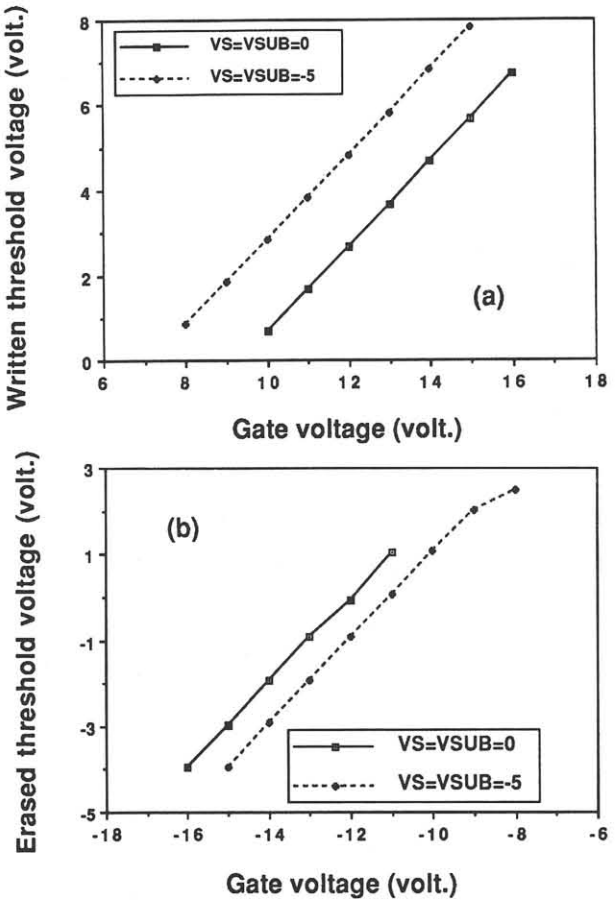


Fig.6 (a)Written and (b)erased threshold voltages as functions of gate voltages with Vs=Vsub=0, and -5V.

Table.II Operational conditions for the cell with Vtw=5V and Vte=0V.

	DRAIN	GATE	SOURCE AND SUBSTRATE
WRITE	GND	12V	-5V
ERASE	GND	-12V	-5V
READ	0.1V	5V	GND

mode device due to over-erasing can be avoided. Moreover, since both gate voltage and negative voltage must be used to activate the programming and erasing, the select transistor can be eliminated[3] and the cell can be further reduced.

The programming and erasing schemes have been tested up to 100 cycles for observing its endurance under this enhanced electric-field stressing conditions[4]. The endurance-test results in Fig.7 show that the threshold window remains unchanged in both cases with and without hot-electron injection.

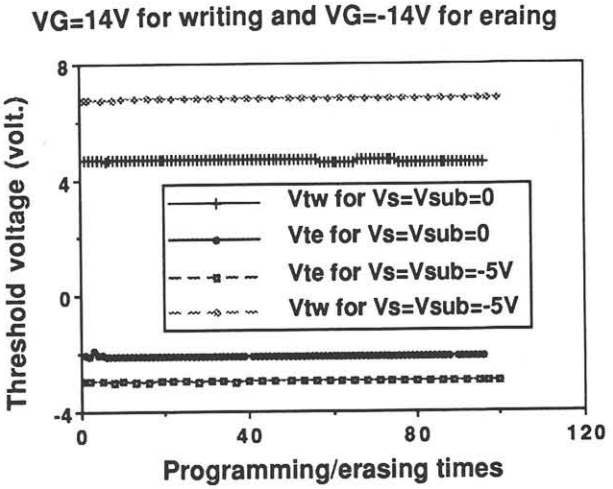


Fig.7 The endurance tests for the write/erase with (Vs=Vsub=-5) and without (Vs=Vsub=0) channel hot-carrier injection.

4. CONCLUSION

It is found from the experimental analysis that a negative voltage applied to source and substrate can reduce the programming and erasing gate voltage magnitudes while keeping the same programmed and erased threshold voltages. The erased threshold voltage can be kept a little greater than 0V, so that a large current flow through the deep-depletion device can be avoided. Moreover, selective programming and erasing operations can be achieved directly without the selection transistor.

ACKNOWLEDGMENT

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