Extended Abstracts of the 1992 International Conference on Solid State Devices and Materials, Tsukuba, 1992, pp. 310-312

A GaAs Junction-Gate FECFET for the Digital Integrated Circuits

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We proposed and fabricated a new GaAs Junction-gate Floated Electron Channel FET(J-FECFET) to fabricate the direct coupled FET logic circuits. By varying the mask stripe width in selective MOCVD, the threshold voltages can be controlled. The enhancement-mode J-FECFET shows the maximum extrinsic transconductance of 350mS/mm with the threshold voltage of -0.1V. The FET with the higher threshold voltage can be made by reducing the mask stripe width. The negligible sidegate effect is observed in the fabricated J-FECFET.

1. Introduction

In order to achieve high speed and low-power GaAs IC's, Direct Coupled FET Logic(DCFL) circuit has been developed[1]. Due to the small logic swing of MESFET's, the threshold voltage of the enhancement-mode MESFET in the DCFL circuit should be precisely controlled. In this respect, the DCFL circuit employing JFET allows larger logic swing than that with MESFET's[2]. In spite of this advantage, logic circuit having junction gate FET's have not been used extensively because of its inherent difficulties in the fabrication process. JFET devices have been usually fabricated using the diffusion techniques of Zn through a mask into the n-type channel to form the p-type gate[3] [4]. The other approachs were attempted by the use of the p-type gate produced with Mg^+ or Zn^+ ion implantation[3] [6]. Even though the shallow junction technique has been developed, we think there was some performance degradation due to its unwanted side-wall parasitic capacitances produced at the p^+-layer edges embedded in active layer.

In this report, we describe the new GaAs Junction-gate Floated Electron Channel Field Effect Transistor (J-FECFET) and the applicability of this device on digital integrated circuits. Recently, we reported the FECFET as a candidate transistor for digital integrated circuits[7]. It was pointed out that this device has many advantages such as simple realization of DCFL, reduced sidegate effect and small source resistance etc.. By adding a p^+-layer on the n-layer of the conventional FECFET, it is possible to increase the built-in potential and thus increase the logic swing which is of interest to GaAs digital circuits. Because source and drain ohmic contacts are formed on the n^+-layer by etching away the p^+-layer and the active n-layer using the gate metal as an etch mask, the parasitic gate capacitances can be reduced compared to the conventional JFET as shown in fig. 1.

2. Device Structure and Fabrication

Fig. 1 shows device geometry for a junction-gate FECFET. The p^+-GaAs layer is used to increase the gate built-in voltage. The threshold voltages of the FET's is controlled in a wafer by varying the mask stripe width with constant epitaxial layer thickness and active doping concentration[7]. The device fabrication process is briefly described as follows.

The substrate used in this experiment is LEC-grown Cr doped semi-insulating GaAs (001) wafer. After the slight etching the substrate with H_2SO_4 system and rinsing in deionized water, SiO_2 stripes with various width are patterned on the substrate. The stripe width for the enhancement-mode FET is usually larger than that of the depletion-mode FET. For example, in order to obtain the proper threshold voltage difference between E-mode(Vth=0.1V) and D-mode(Vth=-1V) devices, it is necessary to form the stripe width difference of 0.2μm for the doping concentration of 1×10^{17} cm^{-3}. The sputtered SiO_2 thickness is about 0.05

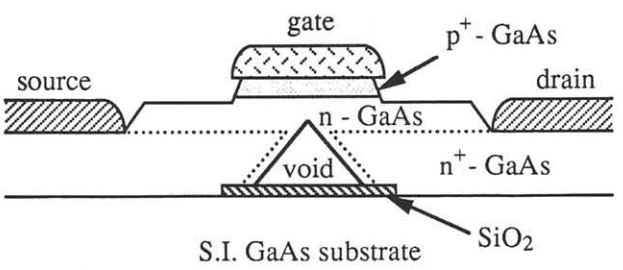

Fig. 1. Cross sectional view of the junction-gate FECFET.

μm and the orientations of the stripe is 20° off from the [1̄10] direction. Then, n^+-layer for source and drain ohmic cantact and n layer for active channel are successively grown. We used the atmospheric-pressure Metalorganic Chemical Vapor Deposition(MOCVD) system for the growth of the layers. Arsine and Trimethylgallium are used as the source materials. The growth rate is about 0.03μm/min at the growth temperature of 650°C. In this case, the thickness of n-layer and n^+-layer and the doping concentration of n-layer are adjusted to produce the desired threshold voltages. The thick n- and n^+-layer give a small sheet resistance of 17Ω/square. After the n- and n^+-layer growth, p^+-layer for the junction formation is consecutively grown. Diethylzinc and silane gas are used as the source of n- and p-type doping, respectively. The gate metal with 2μm length is formed by AuZn/Au evaporation and lift-off. After alloying with rapid thermal alloy system, p^+-layer except gate region is etched away with the gate metal as an etch mask. Ohmic contacts for source and drain is formed by etching the active layer and depositing AuGe/Ni/Au on the n^+-layer. We summarized the designed layer parameters in table 1. The n-layer doping concentration is confirmed from C-V measurement.

Table 1. Epitaxial structure parameters of the fabricated GaAs junction-gate FECFET.

Epitaxial layer	Doping concentration(cm^{-3})	Thickness(μm)
p^+- GaAs	4×10^{19}	0.1
n - GaAs	1.6×10^{17}	0.35
n^+- GaAs	2×10^{18}	0.6

3. Results and Discussions

Fig. 2 shows the current-voltage characteristics of the J-FECFET with the gate of 2μm in length and 100μm in width. The value of maximum extrinsic transconductance(g_m) of 350 mS/mm is obtained at the drain current of 216mA/mm. At V_g =1V and V_d=1V, g_m and output conductance(g_o) were 320mS/mm and 10mS/mm, respectively. These values give the DC voltage gain(g_m/g_o) of 32. The threshold voltage measured at low V_{ds} is -0.1V.

As the mask stripe width is reduced to 1.8μm, the threshold voltage increases up to -1.67V. The output characteristics is shown in the fig. 3. The maximum extrinsic transconductance of the depletion-mode J-FECFET is 150mS/mm at the drain current of 180mA/mm. Further reduction of the mask width to 1.6μm makes the threshold voltage decrease to -4V. The output characteristics of the fabricated J-FECFETs with different threshold voltages are summarized in the table 2.

The current-voltage characteristics of the fabricated p-n diode with the area of 100μm × 100μm is shown in fig. 4, where the Aluminium Schottky diode with

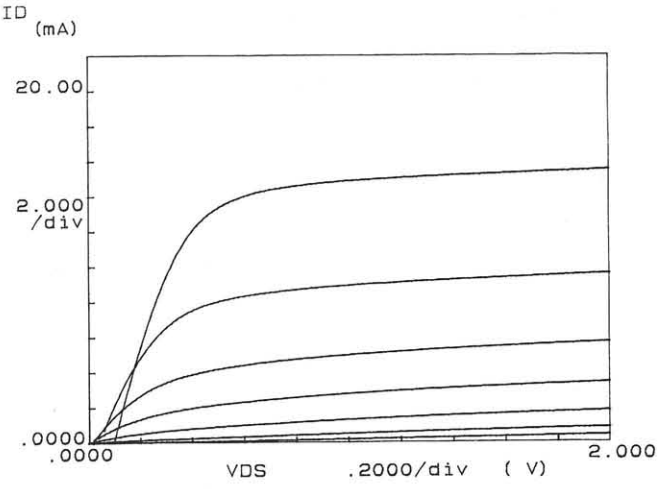

Fig. 2. The current-voltage characteristics of the 2μm × 100μm junction-gate FECFET operated in enhancement-mode. The gate voltage ranges from 1.0V to -0.2V in -0.2V steps.

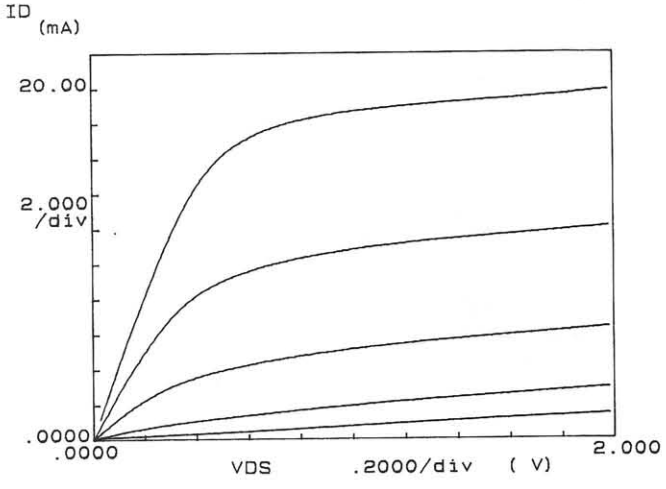

Fig. 3. The current-voltage characteristics of the 2μm × 100μm junction-gate FECFET operated in depletion-mode. The gate voltage ranges from 0.5V to -1.5V in -0.5V steps.

Table 2. Typical device parameters of three junction-gate FECFETs with different threshold voltages. The values within the parentheses are calculated from the threshold voltages.

Stripe width (μm)	Threshold voltage(V)	g_m, max (mS/mm)
2 (2)	-0.1	350
1.8 (1.9)	-1.67	150
1.6 (1.75)	-4.0	150

0.77V Schottky barrier height is also displayed. The reverse breakdown voltage is improved by 4V and the cut-in voltage is slightly increased.

Fig. 5 is the drain saturation current as a function of the sidegate bias for the depletion-mode J-FECFET. The reduction of the drain saturation current is as low as 0.4% even when -10V was applied to the sidegate electrode located 10μm away from the source.

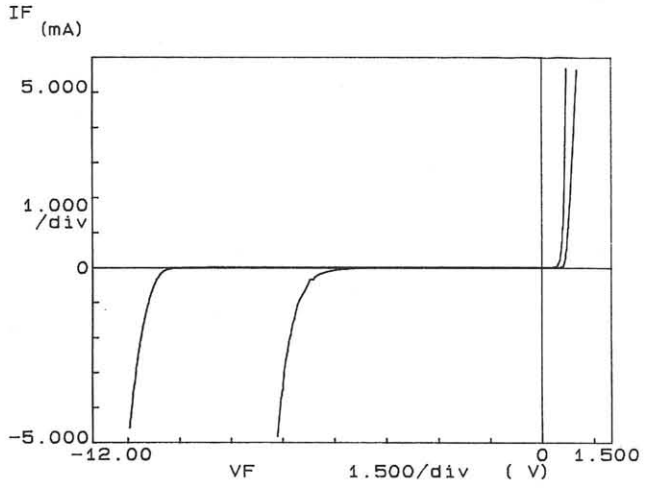

Fig. 4. Forward and reverse current-voltage characteristics of p-n junction(V_{br}=-10V, V_γ= 0.75V) and Al schottky diode(V_{br}=-6V, V_γ=0.6V)

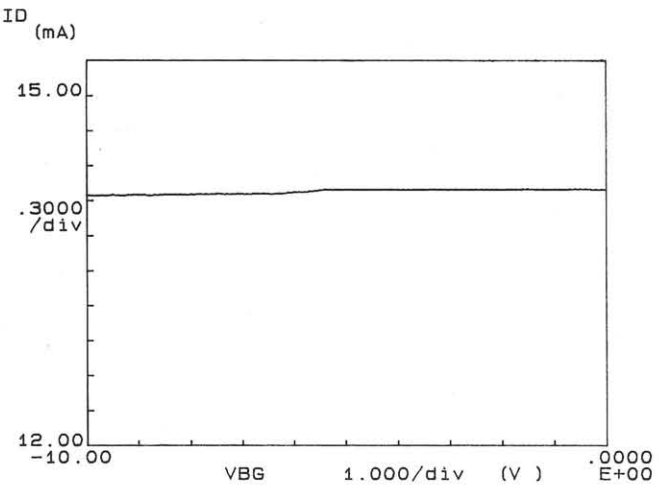

Fig. 5. Drain current versus sidegate voltage characteristics of the junction-gate FECFET

4. Conclusions

We proposed and fabricated a new GaAs junction-gate FECFET for the purpose of the realization of the GaAs direct coupled FET logic circuit. The threshold voltages can be controlled in a wafer by varying the stripe width of the masking silicon dioxide. The enhancement-mode J-FECFET with the threshold voltage of -0.1V demonstrates the maximum extrinsic transconductance of 350mS/mm. As the mask stripe width decreases in the step of 0.2μm, the threshold voltages are lowered to -1.67V and -4.0V. The typical $g_{m,\,max}$ of the depletion-mode J-FECFETs is 150mS/mm. We also shows that the p-n junction in the J-FECFET improves forward and reverse characteristics compared with those of Aluminium schottky diode in conventional FECFET. Finally, it is demonstrated that the fabricated J-FECFET exhibits the negligible sidegate effect. These results show in a clear context that the GaAs junction-gate FECFETs are suitable for the realization of GaAs direct coupled FET logic circuits.

Acknowledgements

The authors would like to thank Dr. Y. S. Kim and Mr. B. S. Park of SAMSUNG Electronics for their helpful discussions and continuous encouragement through this work. This work is supported by SAMSUNG Electronics.

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