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The Impact of Titanium Silicide on the Contact Resistance for Shallow Junction Formed by Out-Diffusion of Arsenic from Polysilicon

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The electrical characteristics of Ti–polycided shallow junctions formed by out–diffusion of As^+ from polysilicon were investigated. Junction depth as shallow as 0.1um and leakage current density as small as $0.4nA/cm^2$ can be easily obtained by this process. Contact resistance measurements show that the presence of a deliberately grown interfacial oxide layer leads to a significantly increase in contact resistance and small values of ρ_c ($4\sim7\times10^{-7}$ Ω–cm^2) can be obtained if the Ti thickness are larger than half of the polysilicon thickness.

1.Introduction.

In the scaled down MOS devices, shallow junctions are needed to minimize device punchthrough, short channel and the other undesirable effects.[1] However, the junction leakage and the source/drain sheet and contact resistances become important consideration.[1,2] The source/drain sheet and contact resistances tend to increase as the junction depth is scaled down. A self–aligned silicide process is usually employed to reduce the source/drain sheet and contact resistances.[3,4] Among them, the self–aligned Ti–silicide is one of the most promising candidates for VLSI devices because of its thermal stability and easy formation of the selective silicide by thermal reaction.[3] For this junction formation technology, contact resistances increase with the increased deposited Ti thickness because of the consumption of the silicon substrate during the silicidation process[1,2]. However, a thicker Ti–silicide layer is still needed to reduce the source/drain sheet resistance and the interconnection routing resistance. To solve the above conflict, a scheme to form the Ti–polycided shallow junction by out–diffusion of impurities from polysilicon is developed.[5] In this scheme, the polysilicon provide not only a convenient source of dopant atoms during forming the junction, but also a silicon source during forming the silicide with no silicon substrate consumed. Also, for this scheme, the implantation damage is confined within the polysilicon layer and a shallow junction depth and a small junction leakage can be expected. In this work, the electrical characteristics of the n^+/p shallow junction formed by out–diffusion of As^+ from polysilicon were studied. Different thicknesses of Ti and polysilicon, different post–silicidation temperatures and different surface treatments to form the junctions were performed.

2.Experiments and Measurements.

The schematic cross section of Ti–polycided n^+/p diodes fabricated with the polysilicon as the solid diffusion source are shown in Fig.1. After the contact window was opened, half of wafers were given an RCA cleaning and half of wafers were given an dilute HF etching. A layer of polysilicon with the thicknesses between 500Å and 1500Å was deposited in a low pressure chemical vapor

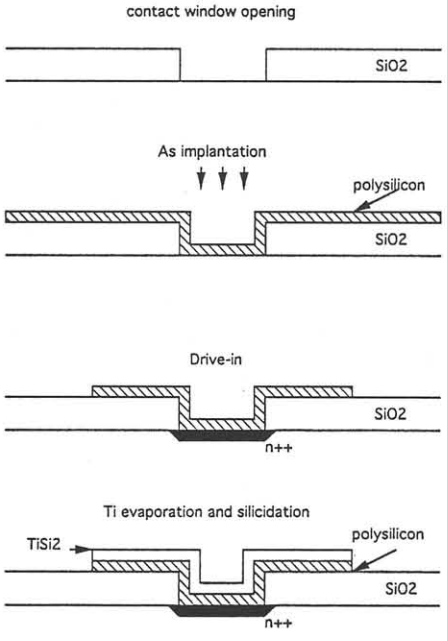

Fig.1 Fabrication steps for Ti–polycided shallow junction.

deposition (LPCVD) system. Then, As^+ with a dose of $1\times10^{16}/cm^2$ at a energy of 80Kev was implanted into the polysilicon and subsequently annealed at 950°C for 15min.. After this, Ti with the thicknesses from 300Å to 1000Å was evaporated by an E–gun system onto the polysilicon film and the wafers were then silicidized process at different thermal cycles.

The junction depth of resulting diodes are measured by secondary ion mass spectroscopy (SIMS) and the junction leakages are measured by a HP–4145 semiconductor analyzer. For contact resistance measurements, the self–aligned vertical Kelvin test resistor structure (SAVTR)[6] is used.

3.Results and Discussions.

Fig.2 shows the SIMS profile of the $TiSi_2/n^+$–p junction. It is seen that an ultra–shallow junction depth (approach to 0.1um) was obtained. It is also seen that an oxygen peak was present at the polysilicon and silicon interface and this indicates that an native oxide layer existed between the polysilicon and the silicon substrate. This interfacial oxide layer would impede the flow of majority carriers and, hence, give rise to a high contact resistance. Fig.3 shows that a small leakage current density (< 0.4 nA/cm^2) was obtained for this contact system. Therefore, the junction formed by this method is not only suitable for the polyemitter contact for bipolar transistors but also suitable for the source/drain contact of half–submicron MOSFETs.

The effect of the interfacial oxide on the contact resistance was investigated with two surface treatments i.e. RCA–treatment and HF–treatment. Fig.4 shows the contact resistances of RCA samples and HF samples in terms the polysilicon thickness for two Ti thicknesses (300Å and 500Å). It is seen that the ρ_c values of RCA samples are generally larger than those of HF samples. This is due to the existence of the relatively thick interfacial oxide of

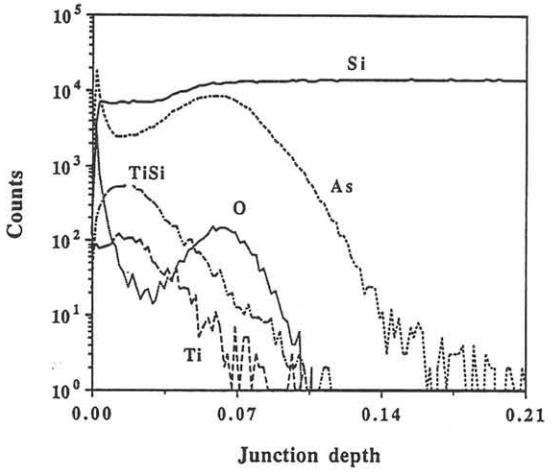

Fig.2 SIMS profile of n^+/p junction. An oxygen peak was present at the polysilicon and silicon interface.

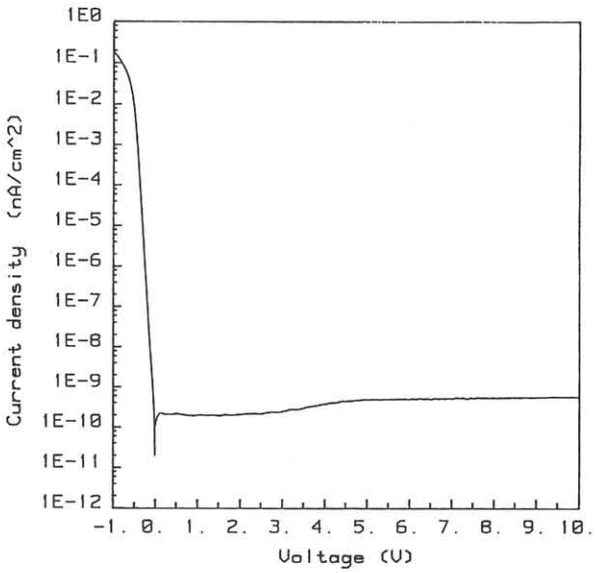

Fig.3 I–V characteristics of n^+/p junction.

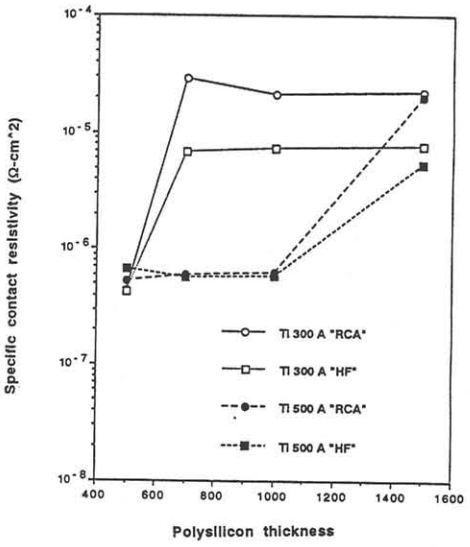

Fig.4 ρ_c vs polysilicon thicknesses with different Ti thicknesses and different surface treatments.

the RCA samples. However, the two ρ_c values approach the same order when the polysilicon thickness is 500Å for the 300Å Ti samples and is 1000Å for the 500Å Ti samples. This is because of polysilicon layers had been consumed completely under these thicknesses and the thin interfacial oxide were broken. Therefore, the contacts were $TiSi_2/n^+Si$ contacts. Hence, to obtain the low ρ_c value ($4\sim7\times10^{-7}$ Ω–cm^2) for both of RCA and HF samples, the Ti thickness should be larger than half of the polysilicon thickness.

Fig.5 shows the ρ_c vs the silicidation temperature with different polysilicon thicknesses for the 300Å Ti samples. It is seen that smaller ρ_c can be obtained for the 500Å polysilicon thickness

samples. This indicates again that the polysilicon of this thickness had been consumed completely during the silicidation process. In addition, for the 500Å polysilicon samples, ρ_c increases slightly with the increased of the silicidation temperature. This is due to the fact that the surface dopant concentration decreases with the increasing silicidation temperature as shown in Fig.6.

Fig.7 is a plot of ρ_c vs the deposited Ti thickness with the different polysilicon thicknesses. For the case of 500Å polysilicon thickness, values of ρ_c in the range of $4\sim7\times10^{-7}$ Ω–cm^2 were obtained for each of Ti thickness and ρ_c increased slightly with the increasing Ti thickness. This is due to the consumption of the silicon substrate. For the cases of 700Å and 1000Å polysilicon thicknesses, larger Ti thickness (>500Å) are needed to obtain the small ρ_c. For the 1500Å polysilicon samples, small ρ_c was obtained only for the 1000Å Ti thickness samples.

4.Conclusion.

It has been shown that the Ti–polycided shallow junctions formed by the out–diffusion of As^+ from polysilicon can have an ultra shallow junction depth (o.1um) and small junction leakage (<0.4nA/cm^2). It has been shown that HF treatment on wafers before polysilicon deposition can improve ρ_c which dropped from $2\sim4\times10^{-5}$ Ω–cm^2 to $5\sim8\times10^{-6}$ Ω–cm^2. To achieve a good contact resistance, the thickness ratio of Ti/polysilicon should be larger than 0.5 so that the polysilicon can be consumed completely by Ti and the interfacial oxide can be broken during the silicidation step. With this, a ρ_c as low as $4\sim7\times10^{-7}$ Ω–cm^2 can be obtained for this junction.

Acknowledgements:

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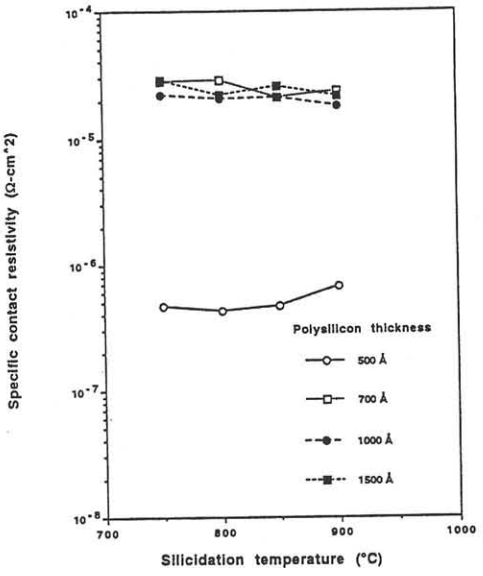

Fig.5 ρ_c vs post–silicidation temperatures for 300Å Ti sample.

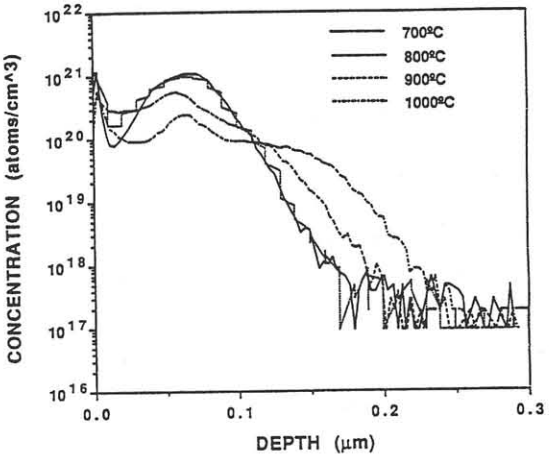

Fig.6 SIMS profile of As^+ concentration for different post–silicidation temperatures.

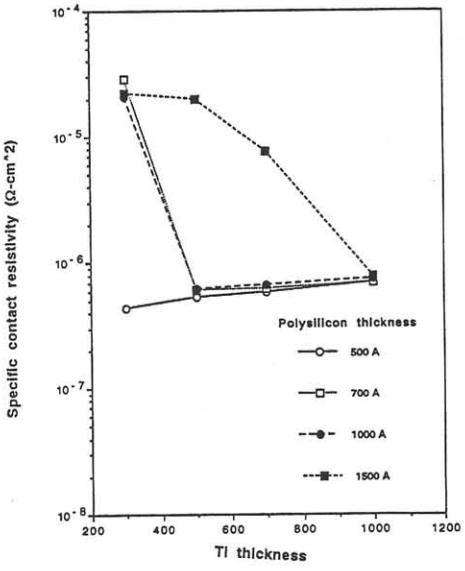

Fig.7 ρ_c vs Ti thicknesses with different polysilicon thicknesses.