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Hemispherical Grained Silicon (HSG-Si) Formation on In-Situ Phosphorous Doped Amorphous-Si Using The Seeding Method

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A new HSG-Si formation technology, "seeding method", which employs Si_2H_6-molecule irradiation and annealing, was applied for realizing 64Mbit DRAMs. By using this technique, grain size-controlled HSG-Si can be fabricated on in-situ phosphorous-doped amorphous-Si electrodes, as well as on non-doped amorphous Si. The new HSG-Si fabrication technology achieves twice the storage capacitance with high reliability for the stacked capacitors.

I. INTRODUCTION

High density DRAM ULSIs require the reduction in memory cell size, resulting in the reduction in cell capacitance. This reduction in capacitance causes very serious limitation to further DRAM integration. In response to this problem, surface area enlargement of storage electrodes is one of the most effective solutions. Several fabrication technologies for uneven surface Si storage electrodes, which form hemispherical-grained (HSG) Si on their surfaces, have been proposed[1,2]. The HSG-Si can successfully increase surface area of storage electrodes. However, it is difficult to control the grain size and density of HSG-Si. Both low-pressure chemical-vapor deposition (LPCVD) method in a narrow temperature range (±3°C)[3], and high-vacuum annealing method of native-oxide-free amorphous-Si[4,5] have difficulties in controlling the nuclei of HSG-Si formation, which are thermally generated on non-doped a-Si surfaces.

Recently, a new HSG-Si formation technology, "seeding method", has been proposed[6]. This method employs Si molecular beam deposition and subsequent annealing to form Si microcrystals on clean amorphous Si surfaces. By using this method, the nuclei generation density and grain size can be well controlled by changing deposition time of Si molecular beam and annealing time after nuclei generation.

In the present work, we have developed HSG-Si capacitor by applying the "seeding method" with Si_2H_6-molecule beam irradiation and annealing[7]. By using this technique, the electrodes with grain size-controlled HSG-Si can be fabricated on in-situ-phosphorous-doped amorphous-Si (P-doped a-Si) electrodes, as well as on non-doped amorphous Si, resulting in effective increase in surface areas. The proposed capacitor electrode has a sufficiently high reliability to be utilized in 64Mbit-DRAMs.

II.EXPERIMENTS

Non-doped a-Si and P-doped a-Si films with completely flat surfaces were formed by LPCVD on SiO_2/Si substrate with contact holes. The concentration of phosphorous in the P-doped a-Si films were $3x10^{20}$ /cm^3. P-doped and non doped a-Si for storage electrodes were patterned by lithography and reactive ion etching. Native oxides on the electrodes were removed by etching with diluted HF solution. For the formation of HSG-Si, the a-Si electrodes were irradiated by Si_2H_6 molecules at 580°C and was subsequently annealed in a high vacuum at the same temperature using UHV-CVD (ANELVA, SRE612). After HSG-Si formation, the non-doped HSG-Si storage electrodes were implanted by 70 KeV arsenic (As) ions with the dose of $1x10^{16}$/cm^2. For activating phosphorous ions electrically, the electrodes were annealed at 800°C in a furnace. SiO_2/Si_3N_4 double layer dielectric films of 6 nm SiO_2-equivalent thickness were employed as capacitor dielectric films. Upper electrodes of polycrystalline-Si was formed by LPCVD followed by thermal phosphorus diffusion.

Surface areas of the storage electrodes were estimated by measuring capacitance values of the stacked capacitors. The electrical reliability was evaluated by measuring leakage-current and breakdown-field distribution of 250,000 stacked capacitor arrays. The surface morphologies of the Si storage electrodes were observed by scanning electron microscopy.

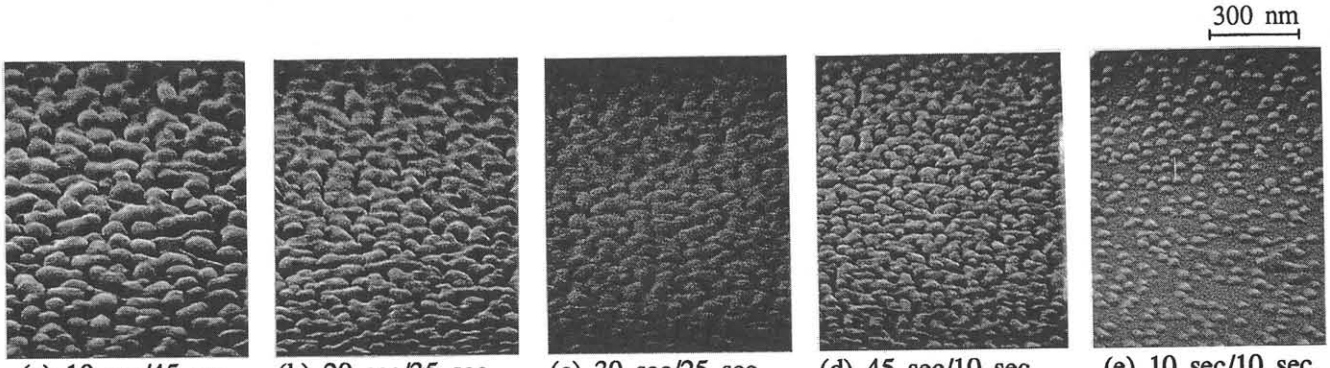

Figure 1 SEM micrographs of Si film surface morphologies after Si_2H_6-molecule irradiation and annealing.

III. RESULTS

Figure 1 shows surface morphologies of Si films which were irradiated with Si_2H_6-molecules at 580°C. The Si_2H_6 irradiation times and the annealing times after Si_2H_6 irradiation were : (a)10sec/45sec, (b)20sec/35sec, (c)30sec/25sec, (d)45sec/10sec and (e)10sec/10sec. The average diameters of HSG-Si formed in these conditions were (a)800Å, (b)600Å, (c)400Å, (d)300Å (e)300Å. High density hemispherical grains of small sizes were obtained after long-period Si_2H_6 irradiation followed by short-period high-vacuum annealing. The large size grains were obtained after short-period Si_2H_6 irradiation followed by long-period annealing. Figs.1 (a) and (e) show that the grain size of HSG-Si can be controlled by changing the annealing time after irradiation of Si_2H_6-molecules. Figs.1 (d) and (e) show that the density of HSG-Si depends on the Si_2H_6 irradiation time. By the new "seeding method", nuclei were formed selectively on the a-Si electrodes by irradiating Si_2H_6-molecules in a wide temperature range, lower than 600°C, in which thermal nucleation did not occur.

Figure 2 shows surface morphologies of storage electrodes with HSG-Si before and after ion implantation. Before ion implantation, the electrode surface was entirely covered with HSG-Si whose diameter was 300Å. During ion implantation, the top surface of electrodes was smoothed by ion sputtering. Therefore, the ion implantation is not suitable for doping HSG-Si electrodes.

When P-doped a-Si films were used for HSG-Si formation by the high vacuum annealing method, HSG-Si was not formed on the electrode surface, but whole electrode was poly-crystallized. This is because the surface recrystallization temperature of P-doped a-Si film is higher than that of the bulk crystallization temperature.

Figure 3 shows the surface morphologies of the P-doped a-Si electrodes after HSG-Si formation (P concentration : $3x10^{20}/cm^3$). By using the new "seeding method", Si_2H_6-molecules, supplied to P-doped a-Si surfaces, play the role of nucleation centers for HSG-Si formation below the temperature of thermally nucleation. The surface morphology was

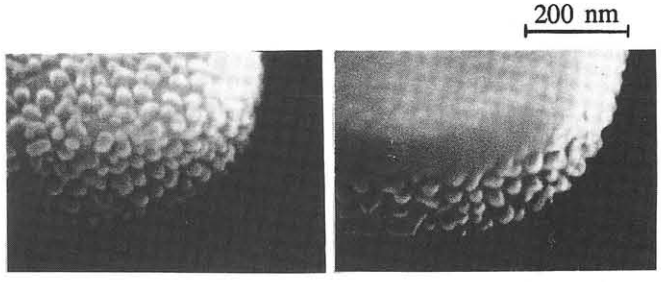

Figure 2

SEM micro graphs of storage electrodes with HSG-Si before and after ion implantation.

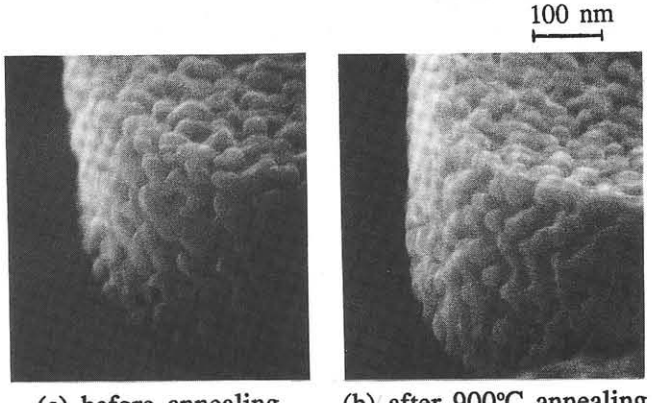

Figure 3

SEM micrographs of HSG-Si formed on P-doped a-Si before and after annealing for activation(600 μΩ cm)

stable after furnace annealing for phosphorous activation. The resistance of HSG-Si electrodes were 600 μΩ cm. The shape and density of HSG-Si on P-doped a-Si was the same as the HSG-Si formed on non-doped a-Si.

Figure 4 shows the capacitance-voltage characteristics of stacked capacitors with respect to the top and the side capacitances. By using the "seeding method" for P-doped a-Si electrodes, the capacitances for both the top and side electrodes increased twice as much as that of conventional electrode. On the other hand, HSG-Si electrodes formed by ion-implantation increased only 1.4 times for the top capacitance. Since the capacitance with the HSG-Si electrode did not change with applied voltages, the depletion layer was not generated.

Figure 5 shows the current-voltage characteristics of 6.0nm-SiO_2-equivalent-thick SiO_2/Si_3N_4 composite films formed on 250,000 stacked capacitor electrodes with 300Å-diameter HSG-Si. The leakage current density of $1x10^{-8}$ A/cm^2 was obtained at cell plate voltages of +2.3V and -2.1V. This value permits sufficient margins for half-3.3V device operation.

Figure 6 shows breakdown-field distributions of 6.0nm-dielectric films formed on 250,000 HSG-Si electrodes. The peak of the breakdown-field distribution is sharp and the breakdown failure in low electric fields is not observed.

VI.CONCLUSION

Stacked capacitors with HSG-Si was formed by using a new HSG-Si formation technology, "seeding method", by employing Si_2H_6-molecule irradiation and annealing. With this technique, surfaces of P-doped a-Si electrodes can be entirely covered with HSG-Si of controlled grain size. By applying the HSG-Si film, formed by the new method, to the storage electrodes of stacked capacitors, twice the storage capacitance and high reliability are obtained. The increase of the capacitance makes it possible to reduce the height of the storage electrode. This technique is applicable to the fabrication process of 64M bit and larger DRAMs.

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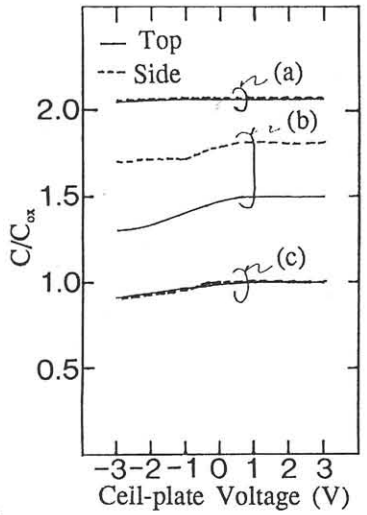

Figure 4

Capacitance-Voltage characteristics.
(a) HSG-Si on in-situ P-doped Si electrodes.
(b) After I/I to non-doped HSG-Si electrodes.
(c) After I/I to non doped conventional electrodes.

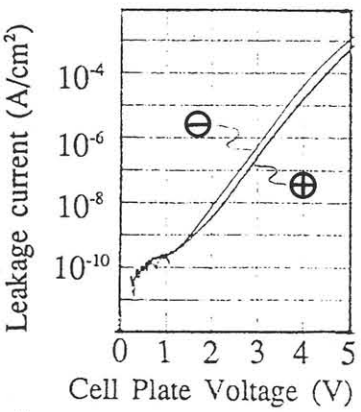

Figure 5

Current-voltage characteristics.

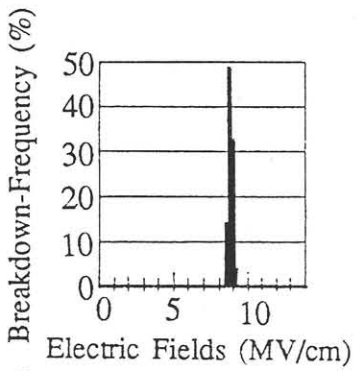

Figure 6

Breakdown-field distributions.

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