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Fabrication of a SiGe-Channel MOSFET Containing High Ge Fraction Layer by Low-Pressure Chemical Vapor Deposition

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A method for growing the high quality strained epitaxial heterostructure as well as the fabrication of $Si_{1-x}Ge_x$-channel pMOSFET containing a high Ge fraction layer have been investigated. It is found that lowering deposition temperature of the $Si_{1-x}Ge_x$ and Si capping layers is necessary with increasing Ge fraction in order to prevent an island growth of the heterostructure. Using optimized $Si/Si_{1-x}Ge_x/Si$ heterostructures with flat surfaces and interfaces, high performance $Si_{0.5}Ge_{0.5}$-channel pMOSFET has been achieved with the large mobility enhancement of about 70% at 300K and over 150% at 77K compared with those of MOSFET without $Si_{1-x}Ge_x$-channel.

1. INTRODUCTION

The growth of $Si/Si_{1-x}Ge_x/Si$ heterostructure at low temperatures has attracted interest for utilizing the improved hole mobility in MOS devices[1-3] as well as in heterojunction bipolar transistors[4]. As growth method, CVD offers many advantages, such as high throughput, in-situ doping and selective deposition. Recently, improvements in the quality of gases and CVD equipment enabled low-temperature epitaxial growth processing[5-8]. For excellent $Si_{1-x}Ge_x$-channel pMOSFET's, high Ge fractions in the strained $Si_{1-x}Ge_x$ layer are necessary. But devices with an expected good performance has been fabricated only for $Si_{1-x}Ge_x$ layer with x around 0.25 or less, deposited by CVD[1,2]. In this work, a method for growing the high quality strained epitaxial hetero-structure as well as the fabrication of $Si_{1-x}Ge_x$ -channel pMOSFET containing a high Ge fraction layer as shown in Fig.1 have been investigated.

2. EXPERIMENTAL

In the heterostructure growth, an ultraclean hot-wall low-pressure CVD system[7] was used. In order to minimize air-contamination in the reactor during the wafer load and unload, a N_2 purged transfer chamber was combined with the reactor inlet. In order to avoid any contamination from the exhaust line, the wafers were transported into the reactor at a reactor temperature of about 100°C under ultraclean N_2 atmosphere through the transfer chamber[8]. While purging with high-purity H_2, the reactor was heated up to the deposition temperature. During vacuum pumping, purge gas was always flowing. All three layers of $Si/Si_{1-x}Ge_x/Si$ sandwich are grown by thermal decomposition of SiH_4 and GeH_4. The typical process sequence for the heterostructure growth is shown in Fig.2. The substrates used were $2x10^{15}cm^{-3}$ n-type wafers with mirror polished (100) surfaces. By Si buffer layer deposition at 750°C, oxygen and carbon pile-ups at the interface between the deposited layer and the Si substrate can be reduced below $5x10^{11}cm^{-2}$. On the $Si_{1-x}Ge_x$ and Si capping layer depositions, the deposition pressure was about 25 Pa,

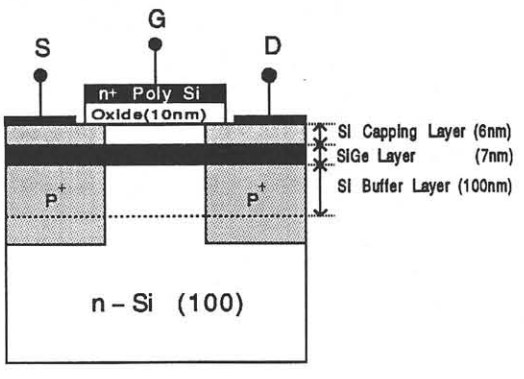

Fig.1. Schematic cross section of $Si_{1-x}Ge_x$-channel MOSFET.

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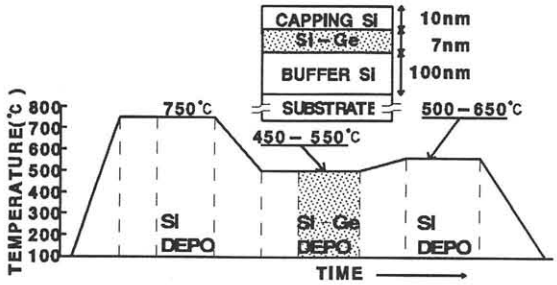

Fig.2. Typical process sequence for $Si/Si_{1-x}Ge_x/Si$ heterostructure growth.

and partial pressure ranges of SiH_4 and GeH_4 were 1–1.4 and 0.03–0.75 Pa, respectively, with H_2 or Ar as a carrier gas. The $Si_{1-x}Ge_x$ layer and Si capping layer were deposited at very low temperatures.

Next, the MOSFET's with a 100μm gate length and 300μm width were fabricated on the $Si(10nm)/Si_{1-x}Ge_x(7nm)/Si$ heterostructures using self-aligned Si gate process. The $Si_{0.8}Ge_{0.2}$ and $Si_{0.5}Ge_{0.5}$ and Si capping layers were formed at 500°C, while $Si_{0.3}Ge_{0.7}$ layer was formed at 450°C. A 700nm field oxide was formed at 400°C by CVD. A 10nm gate oxide was thermally grown by wet oxidation at 700°C. Then, in-situ phosphorus doped n^+ polysilicon was deposited. The source/drain was formed by B^+ implantation ($1.2x10^{15}cm^{-2}$ at 25keV). All anneal processes were performed at temperatures below 700°C.

3. RESULTS AND DISCUSSION

3.1 $Si/Si_{1-x}Ge_x/Si$ heterostructure growth with flat surfaces and interfaces for high Ge fraction

At a higher Ge fraction, it is considered that the heterojunction is degrading by island growth as

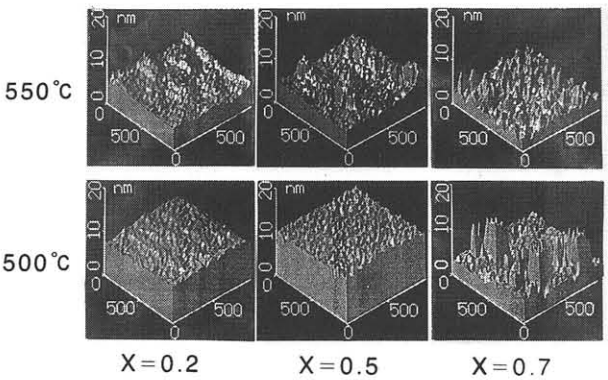

Fig.3. STM surface morphology of $Si(10nm)/Si_{1-x}Ge_x(7nm)/Si$ heterostructures, where the $Si_{1-x}Ge_x$ and the Si capping layers were deposited at 500 and 550°C. The deposition rates of $Si_{0.8}Ge_{0.2}$, $Si_{0.5}Ge_{0.5}$ and $Si_{0.3}Ge_{0.7}$ layers at 500°C were 0.46, 4.6 and 22nm/min, and those at 550°C were 9.7, 17 and 28nm/min and those at 500 and 550°C for the capping layers were 0.11 and 0.43nm/min, respectively.

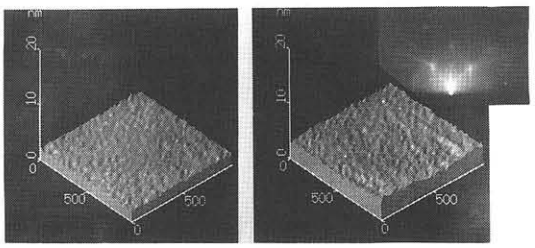

Fig.4. STM surface morphology and electron diffraction pattern of $Si(10nm)/Si_{0.3}Ge_{0.7}(7nm)/Si$ heterostructure, where the $Si_{0.3}Ge_{0.7}$ and Si capping layers were deposited at 450 and 500°C, respectively. the deposition rate of $Si_{0.3}Ge_{0.7}$ layer was 3.7nm/min.

well as by generation of misfit dislocations due to the larger mismatch between the Si and $Si_{1-x}Ge_x$ layers[9]. Therefore, the growth of $Si/Si_{1-x}Ge_x/Si$ heterostructure with flat surfaces and interfaces for high Ge fractions were investigated. The influence of the deposition temperature of the $Si_{1-x}Ge_x$ and Si capping layers, and the Ge fraction in the heterostructure on the surface morphology is shown in Figs.3 and 4. It is found that a higher temperature during $Si_{1-x}Ge_x$ and Si capping layer depositions results in a rough surface, with increasing Ge fraction. The surface roughness, obtained for the heterostructures containing the $Si_{1-x}Ge_x$ layers with x=0.2, 0.5, and 0.7 deposited at 550, 500, and 450°C, respectively, is the same as that of the substrate (average surface roughness R_a < 0.4nm). It has been reported that the mobility of MOS devices with a $Si_{0.6}Ge_{0.4}$-channel is lower than that with a $Si_{0.7}Ge_{0.3}$-channel, where both heterostructures were grown at around 600°C[1]. This fact could be caused by island growth of the $Si_{0.6}Ge_{0.4}$ layer. Our results mentioned above clearly show that lowering the deposition temperatures of the $Si_{1-x}Ge_x$ and the Si capping layers is necessary with increasing Ge fraction to prevent an island growth of the heterostructure. On the fabrication of $Si_{1-x}Ge_x$-channel MOSFET, it was also confirmed that the generation of surface roughness of the heterostructure with x=0.7 did not occur by capping layer deposition and annealing at 550°C, and by wet oxidation for 1 hour at 700°C after the capping layer deposition. The degradation of Ge profile in the channel region was not observed by the above processing within the detection limit of XPS.

3.2 $Si_{1-x}Ge_x$-channel MOSFET characteristics

The threshold voltages of MOSFET's with x=0, 0.2, 0.5 and 0.7 without island growth were −1.3, −1.1, −0.82 and −1.0 V at 300K, respectively, as shown in Fig.5. The threshold voltage can be strongly

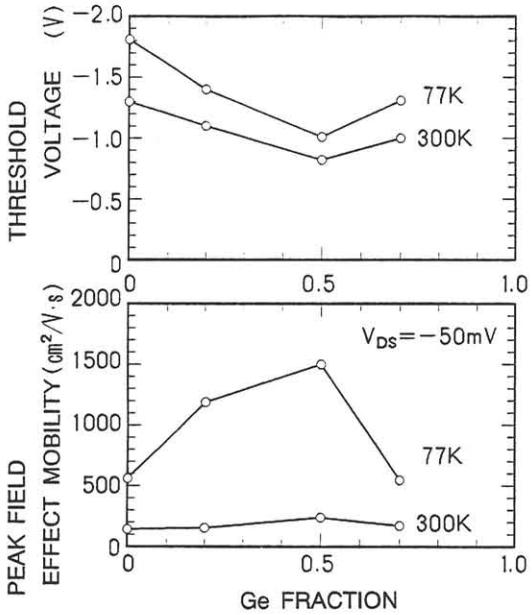

Fig.5. Threshold voltage and peak field effect mobility vs. Ge fraction. The $Si_{0.8}Ge_{0.2}$ and $Si_{0.5}Ge_{0.5}$ and Si capping layers were formed at 500°C, while $Si_{0.3}Ge_{0.7}$ layer was formed at 450°C, to prevent an island growth.

related to the band gap of $Si_{1-x}Ge_x$ layer. The $Si_{0.5}Ge_{0.5}$-channel MOSFET has the largest drain current as shown in Fig.6, the highest peak field effect mobility, and the large mobility enhancement of about 70% at 300K and over 150% at 77K compared with those of MOSFET without $Si_{1-x}Ge_x$-channel (Fig.5). Such mobility enhancement is excellent compared with that reported by other investigators[1-3]. The subthreshold slopes (about 80 mV/decade at 300K and 30 mV/decade at 77K) of the $Si_{0.5}Ge_{0.5}$-channel MOSFET were the same as those of MOSFET without $Si_{1-x}Ge_x$-channel, as shown in Fig.7. The anomalous threshold voltage and mobility of $Si_{0.3}Ge_{0.7}$-channel MOSFET are considered to be caused by the generation of misfit dislocations due to thicker thickness than the critical one. It was also found that $Si_{0.3}Ge_{0.7}$-channel MOSFET with island growth at 500°C has the markedly poor characteristics. About the improvement of MOSFET's with x around 0.7, further investigations are necessary.

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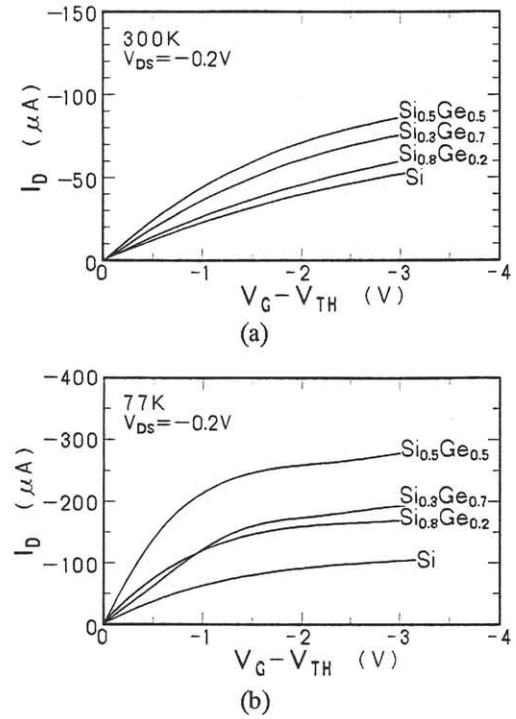

Fig.6. Drain current vs. gate voltage at (a)300K and (b)77K.

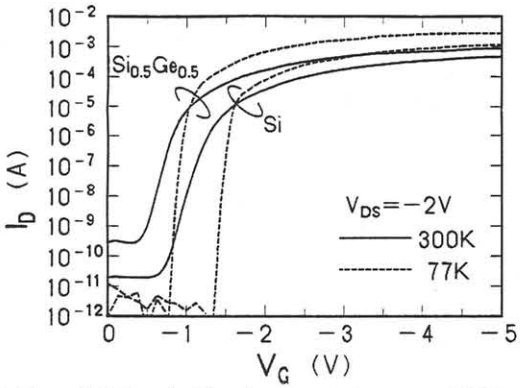

Fig.7. Subthreshold characteristics at 300K and 77K.

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