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Low-Temperature Furnace-Annealed Aluminum-Gate MOSFET for Ultra-High-Speed Integrated Circuits

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Arsenic-implanted self-aligned Al-gate MOSFET's have been successfully fabricated by employing ultra-clean ion implantation technology. The use of ultra high vacuum ion implanter and the suppression of the high-energy-beam-induced metal sputter contamination have enabled us to form low-leakage pn junctions by furnace annealing at a temperature as low as 450°C. The fabricated Al-gate MOSFET's have exhibited good electrical characteristics, thus demonstrating a large potential for application to realizing ultra-high-speed integrated circuits.

1. Introduction

From late 80's to 90's, BiCMOS has been playing an essential role in achieving large current driving capability for high-speed integrated circuits. However, with the scaling down of device dimensions down to sub-quarter micron regime, the need for the reduction in supply voltage is limiting the use of BiCMOS. This is due to the non-scalability of p-n junction built-in potential(≈0.7V) that determines the turn-on voltage of bipolar transistors. For this reason, pure CMOS configuration will revive as a main-stream circuitry in the 90's to 2000's. Therefore, it is most essential to make the current driving capability of a MOSFET as large as possible.

Enhancement in the current driving capability of a MOSFET must be pursued by two approaches: the transconductance enhancement per unit gate area and the increase in the aspect ratio W/L. The former requires the increase of C_{OX}(unit area gate capacitance), while the latter requires the formation of a long(large W) and narrow(small L) gate electrode. This results in a severe limitation of a MOSFET speed performance due to the signal propagation delay along a long and narrow gate electrode having the nature of rc distributed-constant transmission line. Polycrystalline silicon is widely used as a gate electrode material due to its compatibility to the already-established silicon processing. However, it can not be used in future ULSI because of its high resistivity of the order of 500μΩcm. The resistivity of a gate electrode material should be as low as possible to minimize the signal propagation delay. Pure aluminum has a resistivity of 2.74μΩcm, more than two orders of magnitude lower than that of polysilicon, being an ideal material for gate electrode. The application of aluminum to the gate electrode material, however, requires low temperature processing much below the melting point of aluminum(660°C) after gate aluminum deposition. In order to form source and drain junctions self-aligned to the aluminum gate, annealing of ion implanted layer needs to be carried out at such low temperatures. The RTA process is not applicable to this purpose because RTA can only reduce the thermal budget by shortening the annealing time but still uses a temperature higher than 1000°C. The annealing temperature must be much lower than 660°C. However, the junctions annealed at such low temperatures exhibited very large reverse bias currents[1,2]. We have studied the origins for the large leakage currents and have succeeded in its reduction by ultra clean implantation technology[3-8]. The purpose of this paper is to report on the application of the newly-developed 450°C annealing process to the fabrication of self-aligned aluminum-gate MOSFET's having very low reverse-current arsenic-implanted n^+p junctions.

2. Ultra-clean ion-implantation and 450°C annealing technology

Michel et al. and Tsukamoto et al. have reported that the leakage current of the ion-implanted pn junction becomes very large when annealing temperature is lowered as shown in Fig. 1 [1,2]. We have found that a trace amount of impurities incorporated during the ion implantation has a profound effect on the integrity of the interface between the ion-implanted layer and the substrate after post-ion-implantation anneal. The poor interface integrity is the primary reason for the large leakage currents of low-temperature annealed junctions because no dopant diffusion occurs during annealing and the defects generated at the interface are existing in the depletion region of pn junction[6]. Oxygen or other contaminant from ambient can be eliminated by making the ion implanter UHV compatible[3]. We also found out that metallic impurity contaminations are caused by the ion-beam-induced sputtering of the chamber wall. Therefore, we have developed an ultra-high-vacuum ion

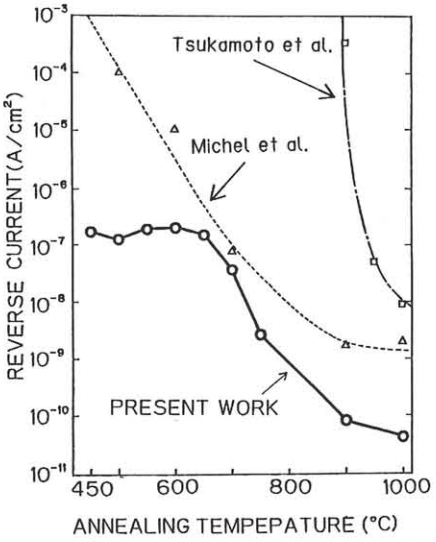


Fig. 1. Reverse bias current of implanted pn junction as a function of the annealing temperature.

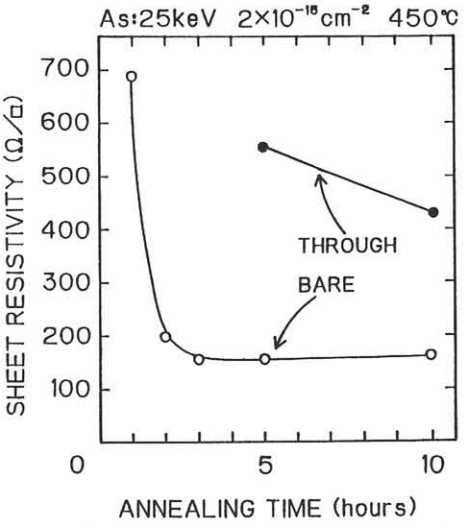


Fig. 2. Sheet resistance of the ion-implanted n^+ layer as a function of the annealing time. The implantation was carried out on the bare silicon surface (open circles) or through 100Å oxide (solid circles).

implanter being equipped with a "sputtering protection board" which is made of silicon and suppresses the sputtering of chamber walls. The data of the reverse-bias leakage-current of n^+p junctions fabricated using this technology are also shown in Fig. 1. A very low reverse current of $\sim 1\times10^{-7}$ A/cm^2 is obtained by conventional furnace annealing at a temperature as low as 450°C.

Figure 2 shows the sheet resistance variation of arsenic ion-implanted and 450°C furnace-annealed layers as a function of the annealing time. The sheet resistance of the sample implanted to a bare silicon surface (open circles) reaches its minimum value of 156Ω□ within three hours. However, for the sample implanted through 100Å oxide(shown by solid circles), the sheet resistance does not decrease even after 10 hours of annealing. By the activated-carrier profile measurement, this is found to be due to the incomplete recrystallization. This delay in the recrystallization of the sample implanted through 100Å oxide can be explained by that oxygen atoms in the oxide are knocked on into the implanted layer and retard the solid phase epitaxial regrowth. Therefore, it is quite essential in the fabrication of aluminum gate MOSFET's to perform source and drain ion implantation to bare silicon surfaces.

Figure 3 shows typical reverse-current voltage characteristics of a 450°C annealed n^+p-junction. Very low reverse-bias current is obtained.

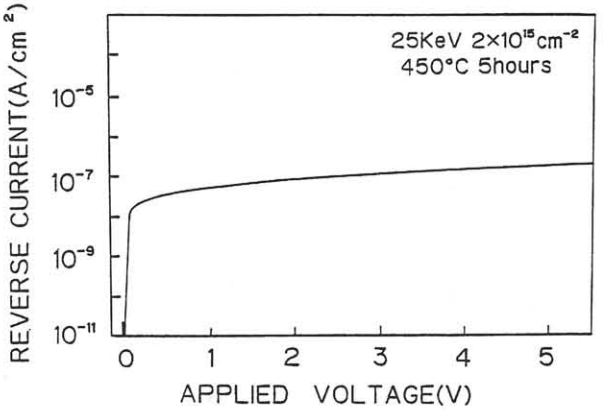


Fig. 3. Typical reverse-current voltage characteristics of a 450°C annealed n^+p-junction.

3. Self-aligned aluminum-gate MOSFET

We have introduced the newly developed 450°C annealing technology to the fabrication of self-aligned aluminum-gate MOSFET's. The fabrication process steps are as follows: P-type (100) wafers of 0.4-0.6Ωcm resistivity were used as a substrate. After forming a 0.6μm-thick field oxide, active areas were opened and a 10nm-thick gate oxide was grown by dry oxidation at 900°C. Pure aluminum film of about 0.6μm-thick was deposited. After patterning gate electrode, the gate oxide on the source and drain surfaces was removed by buffered-HF solution and arsenic ions were implanted on the bare silicon surfaces at 25keV with a dosage of 2×10^{15}cm^{-2}. Then the annealing was performed in an ultraclean nitrogen ambient at 450°C for 8 hours. Contact windows were opened in CVD SiO_2, followed by the forming gas anneal at 400°C for 30 min. Pure aluminum metallization was carried out and no alloying heat cycle was performed after metallization.

Figure 4 shows the photomicrograph of a fabricated MOS transistor and its typical drain current-voltage characteristics are shown in Fig. 5. Parasitic resistance effect at the source and drain due to the ultra shallow junction depth of 500Å is not seen in the characteristics. Threshold voltage of the transistor is 0.144V and subthreshold swing is 71.3mV/decade.

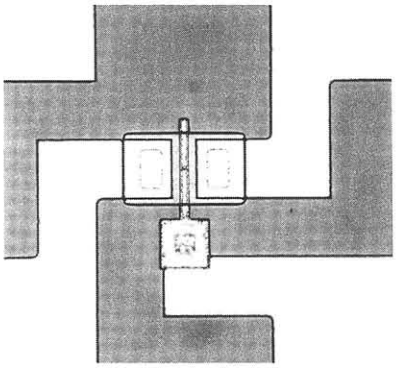


Fig. 4. Photomicrograph of a fabricated self-aligned aluminum-gate MOSFET. The transistor has 3μm gate length and 20μm gate width.

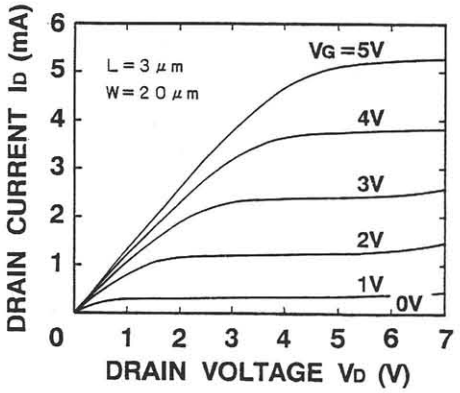


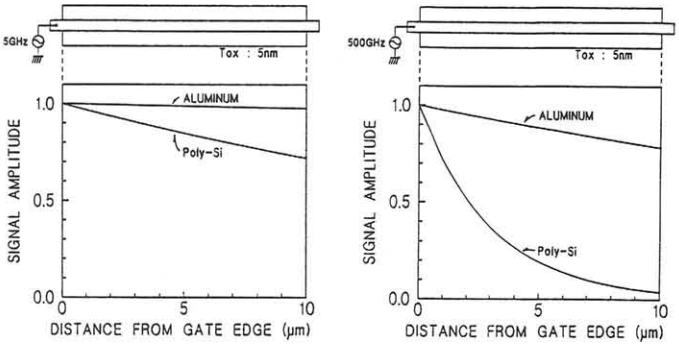
Fig. 5. Drain current-voltage characteristics of self-aligned aluminum-gate MOSFET.

Although the reoxidation process to improve the gate oxide breakdown intensity at the gate edge is essential, this is not possible for Al gate at present. We are now studying the anodic oxidation of Al to use for reoxidation.

Figures 6(a) and 6(b) show the results of calculation for the signal attenuation occurring in the n⁺polysilicon and aluminum gate electrodes. The aluminum gate shows small signal decay even at a extremely high frequency. On the other hand, polysilicon exhibits severe signal decay. From these observations, we can easily recognize that low resistivity gate material is quite essential for the ultra high speed operation. Moreover, the low resistance of metal gate electrode makes it possible to employ high dielectric-constant material as the gate insulator, resulting in further enhanced current driving capability with smaller dimensions(W). This approach, we believe, is the most promising one to realize ultra high speed integrated circuits.

4. Summary

Arsenic-implanted self-aligned Al-gate MOSFET's have been successfully fabricated by employing ultra-clean ion implantation technology. The use of ultra high vacuum ion implanter and the



(a) (b)

Fig. 6. Signal attenuation characteristics along the gate electrode(calculated as lossy distributed-constant transmission line). Calculated results are shown for signals of 5GHz(a) and 500GHz(b). We assume the 5nm thick gate oxide. Bulk resistivities of 500μΩcm and 2.76μΩcm were assumed for n⁺polysilicon and pure aluminum, respectively.

suppression of the high-energy-beam-induced metal sputter contamination have enabled us to form low-leakage pn junctions by furnace annealing at a temperature as low as 450°C. The fabricated Al-gate MOSFET's have exhibited good electrical characteristics, thus demonstrating a large potential for application to realizing ultra-high-speed integrated circuits.

Acknowledgement

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