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Fabrications and Bonding Strengths of Bonded Silicon-Quartz Wafers

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A repeated process set of thinning silicon and annealing was proposed for tight bonding between a silicon wafer and a quartz wafer which have different thermal expansion coefficients. The silicon layers on quartz with the thickness of 2 μm ± 0.5 μm were debonded by the high temperature annealing over 650 C, whereas in the case of thinner silicon layers with the thickness under 0.5 μm ± 0.5 μm, the tensile strengths over 800 kgf/cm^2 were obtained in the temperature range of 700 C ~1100 C.

1. INTRODUCTION

Recent TFT - LCD (Thin Film Transistor - Liquid Crystal Display) uses a - Si layer on glass[1)] or polycrystalline silicon layer on quartz[2)] grown by CVD (Chemical Vapor Deposition). The electron mobilities[3)] in these layers are 0.5 ~ 0.9 and 20 ~ 60 cm^2 v^{-1} sec^{-1}, respectively and are not enough high for future high frequency and high resolution display devices such as an intelligent HDTV. It is also believed that too high density of pins which are connected with outside drivers may not be realized. On the other hand, single crystalline layer of silicon with the mobility of 600 cm^2 v^{-1} sec^{-1}, is expected to solve both the above problems[4)].

Already the bonding mechanisms and the thinning procedures have been reported on silicon/silicon bonding and silicon/oxide bonding with SOI structure[5)]. In this paper, the fabrication process and bonding strength of silicon/quartz wafers are described.

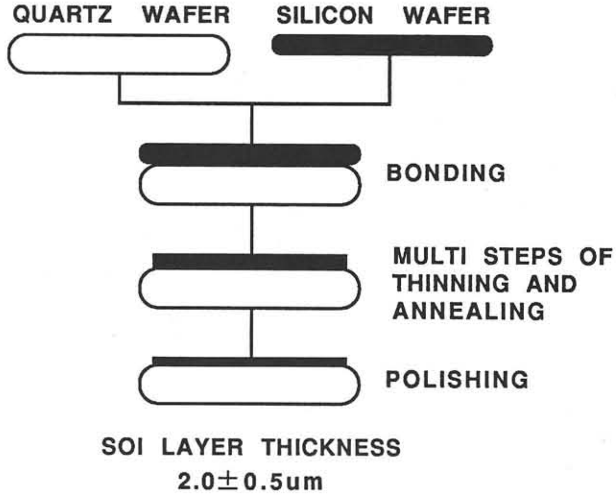

Fig. 1 Schematic of silicon-quartz wafer bonding process with SOI structure

2. EXPERIMENTS

2.1. Bonding and Thinning Processes

Prime quality silicon wafers with (100) orientation and synthetic quartz wafers for photomask with the same diameter of 100 mm and thickness of 525 μm are used. A cleaned silicon and quartz surface stick together by themselves at room temperature strongly, but it is not enough to use a surface grinder to remove the silicon layer of the thickness of almost 520 μm. In order to increase binding strength of silicon and quartz, high temperature annealing is necessary. However, due to the large difference of the thermal expansion coefficients (Si : 2.33 x 10^{-6}, Silica : 0.6 x 10^{-6}), a sticked wafer will be broken over the temperature of 180 C. It is recessary to use a thinner silicon wafer with the thickness of 150 μm, but it is difficult to prepare directly such a thin wafer. The outline of our process is schematically shown in Fig.1. At first the silicon wafers with the thickness of 300μm are used as a starting silicon. After sticking at room temperature, the bonded wafer is annealed at 200 C for 2 hrs. and then etched off at 80 C with a KOH solution by the silicon thickness of 150 μm. After annealing at 300 C, for 2 hrs., the silicon layer is remained by a surface grinder to the thickness of 5 μm and finally polished off by a conventional mechano - chemical polisher to two kinds of thicknesses of 2 μm ± 0.5 μm and 0.5 μm ± 0.5 μm. An oxygen ambient is used for the specimen preparations but a nitrogen ambient is used for the tensile tests for 2hrs. as described in the next section.

2.2. Bonding Strength Measurements

The bonded wafers with thinned silicon layers are diced to 7 x 7 mm^2 specimens for the tensile test after high temperature annealings. 10 pieces and 20 pieces of the specimens from the series of 2 μm + 0.5 μm and from the series of 0.5 μm + 0.5 μm are used, respectively. The schematic structure of a tensile tester (Sebastian V : Quad Group) used for this experiment is shown in Fig. 2 (a).

The cross section of this jig adhered to the silicon layer is 5.7 mm^2. The tensile strength of the adhesive (araldite) is 800 kgf/cm^2. When the bonding strength between silicon and quartz is over 800 kgf/cm^2, separation is occurred as shown in the upper schematic of Fig. 2 (b). The middle schematic shows the fracturing of quartz. The lower schematic means the real binding strengths between silicon and quartz, that is the week bonding for device processes.

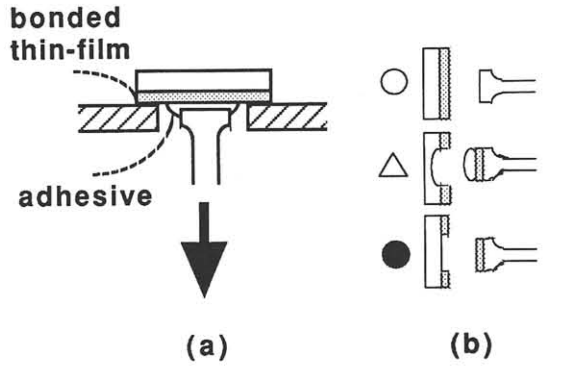

Fig. 2 Schematic of a tensile tester for bonded thin silicon layer (a)

Three seperation modes (b)
Seperation at adheshive (top)
Fracturing (middle)
Seperation at bonded interface (bottom)

3. RESULTS AND DISCUSSIONS

Figure 3 shows the results of the specimens with the thickness of 2 μm ± 0.5 μm on the different temperatures. Over 700 C range, all specimens show the fractures of quartz. It may correspond to the unperfect bonding such as microvoids or high stressed interfaces due to misfit dislocations. Even under 650 C range, the tensile strengths distribute in the lower strength values than that of the adhesive. It is anticipated that the bonding reaction is not proceeded yet due to lower temperature annealing. Figure 4 shows the results of the specimens with the thickness of 0.5 μm ± 0.5 μm. At the temperatures of 700 C and 800 C, almost perfect bonding is obtained under the thickness of 1.0 μm. At the temperatures of 900 C, 1000 C and 1100 C, almost perfect bonding is only obtained under the thickness of 0.5 μm. In the thicker specimens than 0.5 μm, the fractures are occurred. It may be due to dislocation and /or cracking generation. At the

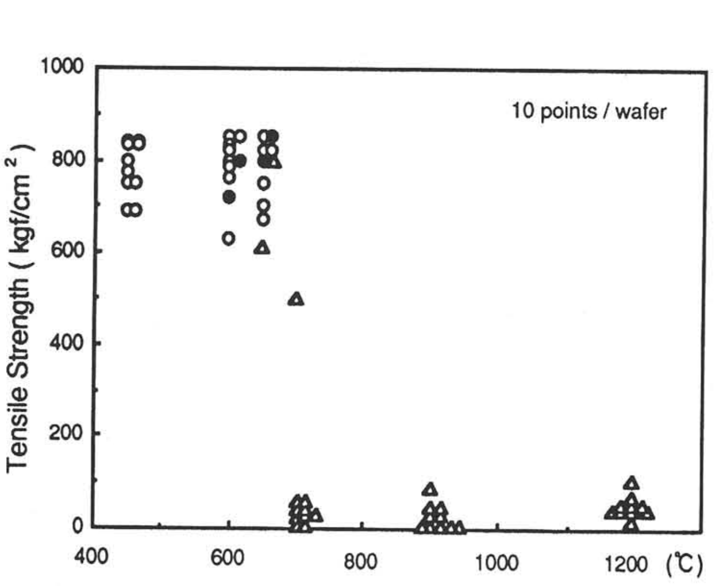

Fig. 3 Temperature dependence of tensile strengths for thick silicon layer (2.0±0.5um)

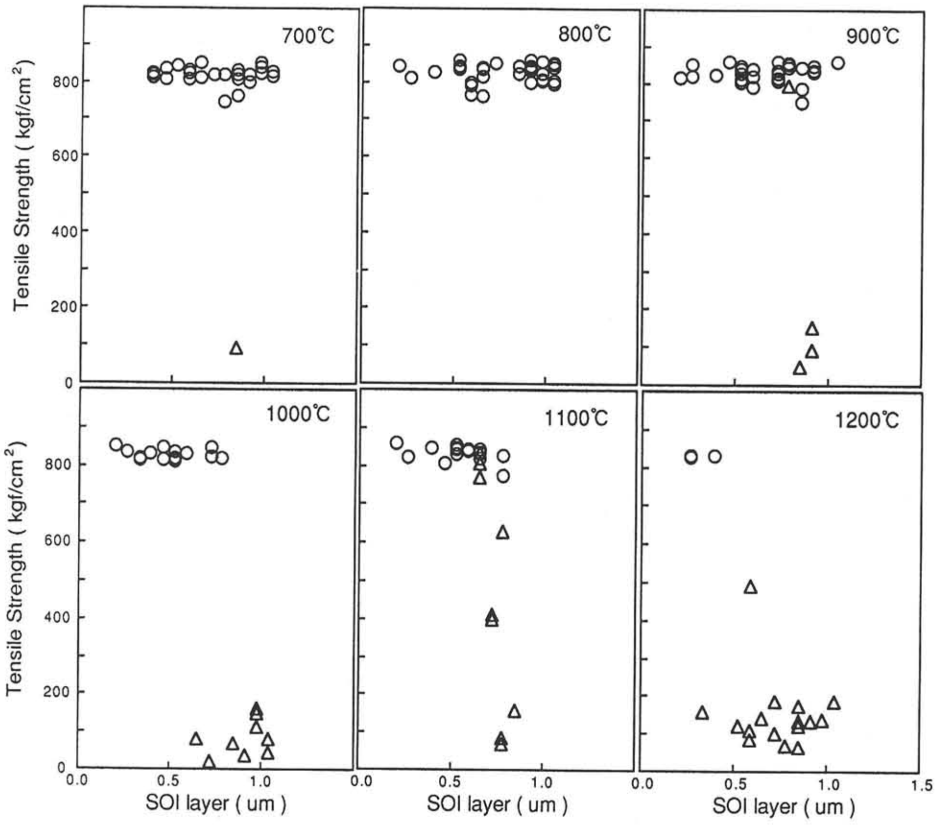

Fig.4 Temperature and silicon layer thickness on tensile strength for thin silicon layer (0.5 ± 0.5um)

temperature of 1200 C, bonding strength decreases. The macroscopic warpage of this wafer is clearly observed. This may be due to the deformation of amorphous quartz at high temperature.

4. CONCLUSION

A repeated process set of thinning silicon and annealing was proposed for tight bonding between a silicon wafer and a quartz wafer which have different thermal expansion coefficients. The silicon layers on quartz with the thickness of $2\ \mu m \pm 0.5\ \mu m$ were debonded by the high temperature annealing over 650 C, whereas in the case of thinner silicon layers with the thickness under $0.5\ \mu m$, the tensile strengths over 800 kgf/cm^2 were obtained in the temperature range of 700 C~1100 C.

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