Extended Abstracts of the 1992 International Conference on Solid State Devices and Materials, Tsukuba, 1992, pp. 650-652

S-II-10

Low Defect Density Low Stress GaAs Grown on Undercut GaAs on Si

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GaAs layer was grown on the UCGAS (undercut GaAs on Si) structure in which the GaAs/Si interface is partly eliminated by the post-growth processing. Dislocation density and the residual stress were reduced to < 5 x 10^5 cm^{-2} and < 2 x 10^8 $dyn \cdot cm^{-2}$, respectively by inserting the SLS(strained-layer supperlattice) and by the TCA (thermal cycle annealing). These improvements are due to the fact that the UCGAS has very small stress and hence is free from the stress-induced-dislocation generation during the cooling after the growth.

1. INTRODUCTION

GaAs grown on Si is very attractive to fabricate the light emitting devices on Si. However, the high density of dislocation has prevented the practical use of these devices.The dislocations act as dark spots, and their density increases during device aging under the influence of the residual stress.[1] The stress is also known to nucleate dislocations during cooling from growth temperature to room temperature after the growth.[2] Therefore, the stress reduction is required not only to increase the device lifetime but also to reduce the dislocation density. We have proposed UCGAS (undercut GaAs on Si) structure to solve these problems.[3-5]

This paper shows that the insertion of the SLS (strained-layer supperlattice) and the TCA (thermal cycle annealing) during the growth of GaAs on the UCGAS extremely reduces both the dislocation density and the thermal stress.

2. EXPERIMENTAL

The UCGAS structure fabricated in the experiment is shown in Fig.1. GaAs and $Al_{0.65}Ga_{0.35}As$ (3 µm-thick) with SLS and TCA were grown on the Si (100) 4° off substrate by MOCVD. The UCGAS structure was then fabricated by selectively etching AlGaAs layer in the lateral direction. The structure was strong enough to endure the process. The 2nd. and the 3rd. MOCVD growth were performed on the fabricated UCGAS. The surface 200 nm was etched away just prior to the growth. The grown GaAs was doped with

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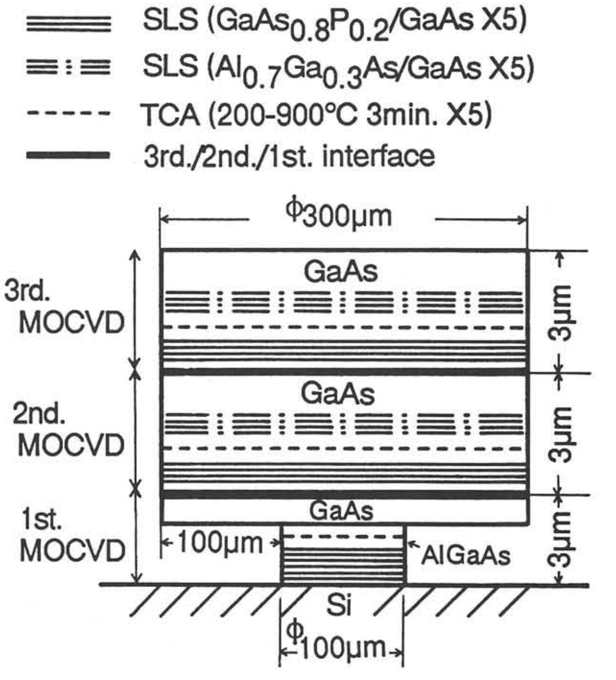

Fig.1 The UCGAS structure used in the experiment.

Si to the electron concentration of 1 x 10^{18} cm^{-3} for the ease of the photoluminescence observation at room temperature. The locations of the SLS and the TCA are shown in Fig.1. The dislocation was characterized by the high magnification (x2400) PLI (photoluminescence image) at room temperature. The 488 nm Ar-ion laser was focused to a diameter of about 40 µm, and the photoluminescence was observed through the longer-wavelength-pass optical filter. The defect-revealing-etching in molten KOH which is difficult to apply in UCGAS due to the strong reaction of Si with KOH is also performed on planar GaAs on Si to compare.

The residual stress was evaluated by the photoluminescence peak wavelength at 55 K. Undoped GaAs layer was grown for this purpose, and the Ar-ion laser was focused to a diameter of 30 µm and scanned in the structure.

3.RESULTS AND DISCUSSION

Examples of the PLI and the etch pit revealed by molten KOH (400 °C, 3 s) at exactly the same location are shown in Fig.2. Most of the etch pits (a',b',c') correspond quite well to the DS's (dark spots) in PLI, however, some of the DS's do not. The DS is originated from the dislocation as well as other non-radiative defects such as impurities, cluster of point defect and dusts. As a result, the DSD (dark spot density) is about 1.5-2.0 times more than EPD (etch pit density). DSD is more important than the EPD to characterize the materials for optical devices.

The PLI's of the surface GaAs after the 1st., the 2nd. and the 3rd. MOCVD growth are shown in Fig.3. The 2nd. and the 3rd. growth were performed on the UCGAS and on the planar GaAs on Si simultaneously. The DSD reduction of the layer grown on the UCGAS after each run is remarkable, and the DSD becomes less than 5 x 10^5 cm^{-2} after the 3rd. growth. On the contrary, the DSD reduction on the planar layer is not significant when it is compared to that of the layer grown on the UCGAS. No crack is formed in the layer grown on the UCGAS even after the 3rd. run where the total layer thickness is 9 µm, while the layer on the planar substrate always contains high density of cracks.

It was also found that the SLS is effective to reduce the defect density

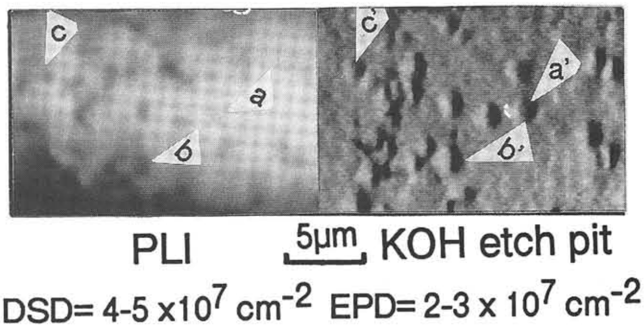

Fig.2 The PLI and KOH etch pits at the same location. The points a,b,c correspond to a',b',c'.

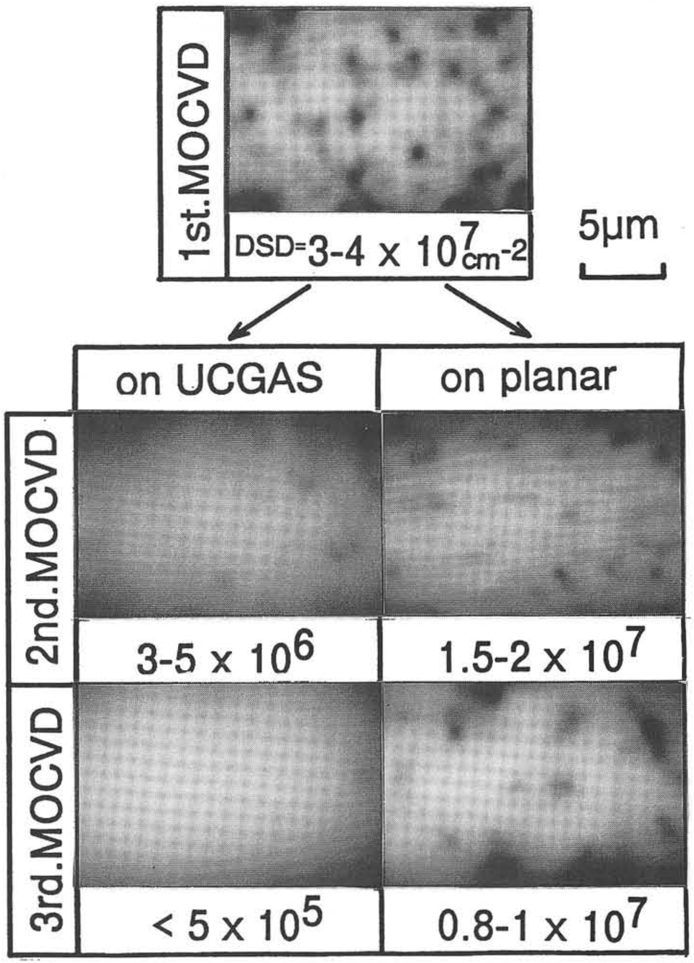

Fig.3 The PLI's of GaAs after the 1st., the 2nd. and the 3rd. MOCVD growth on the UCGAS and on the planar GaAs on Si.

in the layer grown on both the UCGAS and on the planar layer but TCA is not effective on the former. The misfit stress in the SLS change the direction of the dislocation to reduce the dislocation density in the layer grown on it. The TCA also produces stress due to the thermal expansion coefficient mismatch in the planar

GaAs on Si, but this opportunity is not available in the UCGAS making the TCA ineffective in the UCGAS. The other important dislocation generation process is the stress-induced dislocation which is brought about during cooling from growth temperature to room temperature. This mechanism, however, does not exist in the UCGAS since it is free to move making the UCGAS more effective in reducing defect. Further reduction of the dislocation density may be possible by improving the SLS structure.

The photoluminescence spectra at 55 K of undoped GaAs on the UCGAS, planar GaAs on Si and homoepitaxial GaAs are shown in Fig.4. The exciton-related peak splits into two peaks due to the biaxial tensile stress. The peak associated with the $m_j=\pm 1/2$ valence band shifts to a longer wavelength at a rate of -10.4×10^{-9} $meV \cdot cm^{2} \cdot dyn^{-1}$.[6] Therefore, the peak shift with respect to that of the homoepitaxial GaAs gives the stress value in the layer. The planar GaAs on Si has the stress of 2.5×10^{9} $dyn \cdot cm^{-2}$ at 55 K. The peak wavelength of the UCGAS is almost the same as that of

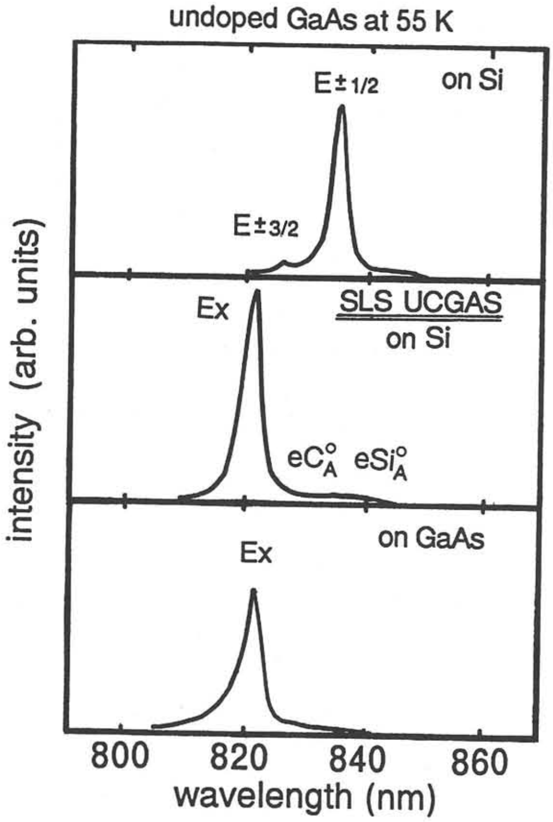

Fig.4 The photoluminescence spectra at 55 K of undoped GaAs on the UCGAS, planar GaAs on Si and homoepitaxial GaAs.

homoepitaxial GaAs. Considering the accuracy of the measurement, the stress in the UCGAS is estimated to be less than 2×10^{8} $dyn \cdot cm^{-2}$. The stress value at room temperature must be even smaller than that at 55 K. The two dimensional scan revealed that the stress in most of the UCGAS part (area; 300 μm^{ϕ} - 120 μm^{ϕ}) is less than 2×10^{8} $dyn \cdot cm^{-2}$. This stress value is small enough, and the area is large enough for the practical device applications.

This structure is successfully applied in fabricating laser diodes and LED's (light emitting diode). The diodes lased in TE mode showing the stress is reduced. The pulsed threshold current of 95 mA for 220 µm long 10 µm wide stripe laser is reasonably low. LED's are operating for more than 2500 h without any significant degradation, and the quantum efficiency increases with decreasing the dislocation density.

4. CONCLUSION

The dislocation density of less than 5×10^{5} cm^{-2} and the residual thermal stress of less than 2×10^{8} $dyn \cdot cm^{-2}$ were simultaneously accomplished by growing GaAs layer with SLS and TCA on the UCGAS structure. These value is small enough for the practical application to the LED. Further dislocation density reduction may be possible by improving the SLS structure.

5. REFERENCES

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