A Study of GaAs Digital ICs on Si Substrates

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The sidegating effect and the operating speed of the circuits on the GaAs/Si substrates were studied using the MESFETs. The decrease of the drain current with the negative sidegate voltage was gradual, however it was small enough for the circuit operation. The propagation delay of the 19-stage DCFL ring oscillator with 0.3 μ m-gate MESFETs was 19.9 ps/gate, which was about 15 % lager than that of the devices fabricated on an undoped semi-insulating LEC GaAs wafer. These characteristics were thought to be affected by the conductive Si substrate.

1. Introduction

GaAs/Si wafers have been proposed as an advantageous material for IC substrates, from the availability of the wafers with a large diameter, a higher thermal conductivity and a superior mechanical strength for fabrication of high speed GaAs ICs.

Since the success of the GaAs epitaxy on Si substrates¹⁾²⁾, many devices and circuits such as MESFETs³⁾. HBTs⁴⁾, ring oscillator⁵⁾, SRAM⁶ 1-kbit have been GaAs/Si fabricated on substrates. However, for the reliable operation and the high integration of the curcuits, it is necessary to evaluate the isolation characteristics between the devices in addition to the operating speed of the circuits.

In this report, the sidegating effect, which directly relates to the isolation characteristics, and the operating speed of the DCFL inverters using the sub-micron gate GaAs MESFETs on Si substrates are described.

2. Device Fabrication

2-inch n⁺-Si wafers with a resistivity of 0.005 ~ 0.02 Ω •cm and an offset angle of 3° from (100) towards [011] were used. GaAs layers were grown on these wafers by the MOCVD 2-step growth technique⁷⁾. The layer structure is shown in Fig.1. For the electrical isolation between the undoped GaAs layer and the Si substrate, the vanadium-doped layer with a high resistivity of 10⁸ Ω •cm⁸⁾ was introduced. No special treatments such as the heat cycle anealing⁹⁾ were applied during the growth in this study.

The sub-micron gate MESFETs were



Fig.1 Schematic cross section of layer structure of GaAs/Si substrate.

fabricated on the undoped GaAs layer by ion implantation process using the self-alignment technique with refractory W-Al gates $^{10)}$.

3. Sidegating Effect

The sidegating effect of the MESFETs on the GaAs/Si was measured by the test configuration shown in Fig.2, where the backside of the Si substrate was grounded. For the GaAs/Si and the semi-insulating undoped LEC GaAs substrates, the dependence of the drain current I_D on the sidegate voltage V_{sc} is shown in Fig.3, as a parameter of the spacing (L_{sc}) between the sidegate and the source. The drain current shows a different behavior for each case; for the GaAs/Si, the drain current decreases gradually with the negative sidegate voltage, while for the undoped LEC GaAs, the drain current abruptly decreases beyond the threshold of the sidegate voltage.

For the undoped LEC GaAs, it was



Fig.2 Test configuration for sidegating effect measurement.



Fig.3 Dependence of drain current on sidegate voltage.

reported that the leakage current from the part of the gate-electrode, which contacts directly on the semi-insulating GaAs surface, to the n^+ region of the sidegate triggers the sidegating effect¹¹⁾; At the sidegate voltage, which is determined by the abrupt increase in the leakage current, the drain current begins to decrease.

The leakage current from the Schottky metal to the n⁺ region of the sidegate was measured for the GaAs/Si substrate, using another test configuration shown in Fig.4(a), where the gate pattern was formed directly on the GaAs epi-layer. The negative bias was applied to the sidegate, and the Schottky metal and the backside of the substrate were grounded. The sidegate current I_{sc} , the Schottky current I_{g-sc} and the substrate current I_{SUB} are shown in Fig.4(b) as a function of the sidegate voltage V_{SG} . The spacing L_{GAP} between the Schottky metal and the n⁺ region was 7.5 μ m. The amount of the sidegate current Isc was almost equal to the substrate current $I_{\text{SUB}},$ while the Schottky current $I_{\text{G-SG}}$ was at most 10^{-9} A, which was almost ten times



- Fig.4 Currents of I_{G-SG} at Schottky metal, I_{SG} at n^+ region, and I_{SUB} at Si substrate are measured, when negative bias of V_{SG} is applied to n^+ ohmic region, and Schottky metal and backside of Si substrate are grounded.
 - (a) Test configuration for measurement.
 - (b) Semi-log plots of Isc-c, Isc, and IsuB versus Vsc.

smaller than other current components. This indicates that most of the electron current from the sidegate flows into the grounded substrate, and consequently, the little electron current from the sidegate reaches the Schottky gate and the current from the Schottky gate into the sidegate, which triggers the sidegating effect, is quite small.

In the case of the GaAs/Si, the explained as can be sidegating effect follows. Because the epi-layer thickness is only 3 μ m, the conductive Si substrate is located near the devices and the electric field from the sidegate almost terminates at the Si substrate. However, in the case of the undoped GaAs layer, a high purity crystal, no screening by the ionized impurities or deep levels occurs. Therefore, the band bending between the sidegate and the channel region is so small that the

electric field from the sidegate can easily modulates the channel potential even if most of the electric field terminates at the Si substrate. As a result, the drain current decreases gradually with the negative sidegate voltage, although the amount of the decrease is small. These characteristics are suitable for the circuit operation.

4. Evaluation of Operating Speed

The DCFL ring oscillators with MESFETs were fabricated on GaAs/Si substrates to evaluate the operating speed of the devices. The fabricated gate length of the MESFETs was 0.3 μ m and the n⁺ regions were surrounded by C⁺ implanted p-layers to suppress the short channel effect.

I-V shows Fig.5 the typical characteristics of the MESFET. Good saturation and pinch-off characteristics are obtained. The maximum trans-conductance was as high as 489 mS/mm. The standard deviation of the threshold voltage over the 2-inch wafer was 35.4 mV at the averaged threshold voltage of -65.9 mV. This deviation was a little larger than that obtained for the devices on an undoped LEC GaAs wafer.

Fig.6 shows the propagation delay versus power dissipation property. At a supply voltage of 2 V, the propagation delay was 19.9 ps/gate, which was about 15 % larger than that of the device fabricated on the undoped LEC GaAs. This delay is thought to be resulted from the additional stray capacitance between the devices and the conductive Si substrate.

5. Conclusion

The sidegating effect of the MESFETs and the speed characteristics of the ring oscillators on the GaAs/Si substrates were studied. It was found that the conductive Si substrate affects the device characteristics. As for the sidegating the drain effect, current decreased with gradually the negative sidegate voltage, however the amount of the decrease was small enough for the circuit operation. This small decrease is thought to be caused by the effect that the electric field from the sidegate modulates the channel region. As for the operating speed of the circuits, the 19-stage DCFL ring oscillator with the 0.3 μ m-gate MESFETs showed the propagation delay of 19.9 ps/gate, which was about 15 % larger than that of the devices fabricated on the undoped LEC GaAs. This delay is thought to be due to the additional stray capacitance between the device and the Si substrate.

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Fig.5 I-V characteristics of 0.3 μ m-gate MESFET on GaAs/Si substrate (Gate width is 10 μ m).



Fig.6 Propagation delay versus power dissipation property of 19-stage DCFL ring oscillator.

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