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InGaP/InGaAs/GaAs Pseudomorphic HEMT DCFL Circuits on Si Substrates

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We fabricated InGaP/InGaAs/GaAs pseudomorphic HEMT DCFL circuits with 0.6 μm gates on 3 inch Si substrates. We grew epitaxial layers by MOVPE. The threshold voltage standard deviation of our E-mode HEMTs was as low as 22 mV and the mean value of their maximum transconductances was 242 mS/mm. The basic propagation delay was 31.3 ps with a standard deviation of 1.7 ps. These characteristics are comparable to those of the same structures and processes using GaAs substrates.

1. INTRODUCTION

HEMT ICs have received much attention since the first High Electron Mobility Transistor (HEMT) was invented[1]. We have already fabricated a 45k gate array and 64k SRAM with excellent characteristics[2],[3]. If we are to produce more complex HEMT ICs, we must improve productivity and develop low-power HEMT devices.

Many researchers expect GaAs on Si technology to provide more complex HEMT ICs. Si can have larger area substrates than GaAs and its thermal conductivity is three times higher. Several studies have fabricated AlGaAs/GaAs HEMTs on Si substrates and show that their performance is comparable to HEMTs on GaAs substrates[4],[5].

Short-channel HEMTs are essential to maintain high speed characteristics under low power operation. The InGaP-based HEMT suffers less from the short-channel effect than a conventional AlGaAs/GaAs HEMT because we can reduce the thickness of the InGaP layer which supplies electrons[6]. Pseudomorphic structures may also contribute to reducing the short-channel effect because of their structural confinement of 2 dimensional electron gas (2DEG).

We decided to fabricate InGaP/InGaAs/ GaAs pseudomorphic HEMTs on 3 inch Si substrates. This paper demonstrates the validity of InGaP-based HEMT DCFL circuits with 0.6 μm gates and on Si substrates.

2. DEVICE STRUCTURE AND FABRICATION

We grew layer structures by MOVPE on 3-inch Si substrates oriented 2 degree off (100) toward [011]. First, we grew a 2 μm GaAs buffer layer using the standard 2-step growth method. We mechano-chemically polished this layer, reducing its thickness to 1 μm. The growth sequence following this mechano-chemical polishing was the same as for GaAs: thick undoped GaAs, 14 nm undoped $In_{0.2}Ga_{0.8}As$, 2.5 nm undoped $In_{0.51}Ga_{0.49}P$, 19 nm Si-doped ($n=1.4\times10^{18}$) $In_{0.51}Ga_{0.49}P$, 14 nm Si-doped ($n=1.4\times10^{18}$) GaAs, 3.5 nm Si-doped ($n=1.4\times10^{18}$) $In_{0.51}Ga_{0.49}P$ etch stop layer, 30 nm Si-doped ($n=1.4\times10^{18}$) GaAs, 3.5 nm Si-doped ($n=1.4\times10^{18}$) $In_{0.51}Ga_{0.49}P$ etch stop layer, 30 nm Si-doped ($n=1.4\times10^{18}$) GaAs. We will report the growth details elsewhere[7].

The device structure and the fabrication process of the InGaP/ InGaAs/GaAs HEMT are almost the same as of conventional AlGaAs recessed-gate HEMTs[8]. Figure 1 is a cross section of the device structure. We used a double-etch-stop process and formed E-mode and D-mode recessed-gate HEMTs at the same time. Selective GaAs (AlGaAs) dry etching can be used for selective GaAs (InGaP) dry etching. It is easy to form gate lengths of 0.6 µm by g-line photo-lithography techniques.

3. RESULTS AND DISCUSSIONS

Table 1 compares the static device characteristics of HEMTs on Si and GaAs substrates. Their layer structures and fabrication processes were the same and done at the same time. As you can see, mean maximum transconductance of E mode HEMTs on Si substrates is almost equal to those for GaAs substrates. The K-value, however, is slightly smaller with Si than with GaAs. This is probably because the 2DEG mobility of 3700 cm/Vs is smaller than the mobility of 5000 cm/Vs with GaAs. Although the threshold voltage standard deviation on Si substrates of 22 mV is larger than the 6 mV for GaAs substrates, it is sufficient for IC operation.

We measured drain current, Ids, versus gate-to-source voltage, Vgs, of E-mode HEMTs on Si and on GaAs with linear and semi-log scales (fig. 2). The drain-to-source voltage, Vds, was 1V. You can see from figure 2(a), which has a linear scale, that with both HEMTs Ids is directly proportional to Vgs in the operating region of DCFL circuits. This is characteristic of HEMTs. In the subthreshold region, both Ids curves show exponential dependence on Vgs (fig. 2(b)). Calculated subthreshold swing, S, of E mode HEMTs on Si is 83.7 mS/decade and on GaAs is 75.8 mS/decade. It is thought that pseudomorphic structures make both values fairly good. The swing of the device on Si is somewhat larger than of that on GaAs. The capacitance of the Si substrate is the main reason that the swing is worse with Si than

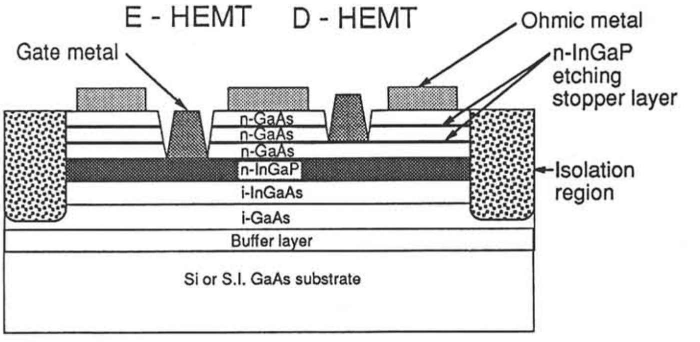

Fig. 1 Cross section of InGaP/InGaAs/GaAs HEMTs.

Table 1 Comparison of Static characteristics of HEMTs with 0.6 µm gates on Si and on GaAs. Values in parentheses are standard deviations.

	on Si		on GaAs	
	E	D	E	D
Vth (V)	0.113 (0.022)	-0.859 (0.102)	0.171 (0.006)	-0.753 (0.010)
K (mS/Vmm)	324 (15)	184 (14)	371 (8)	265 (5)
gm (mS/mm)	242 (7)	211 (8)	236 (1)	224 (3)

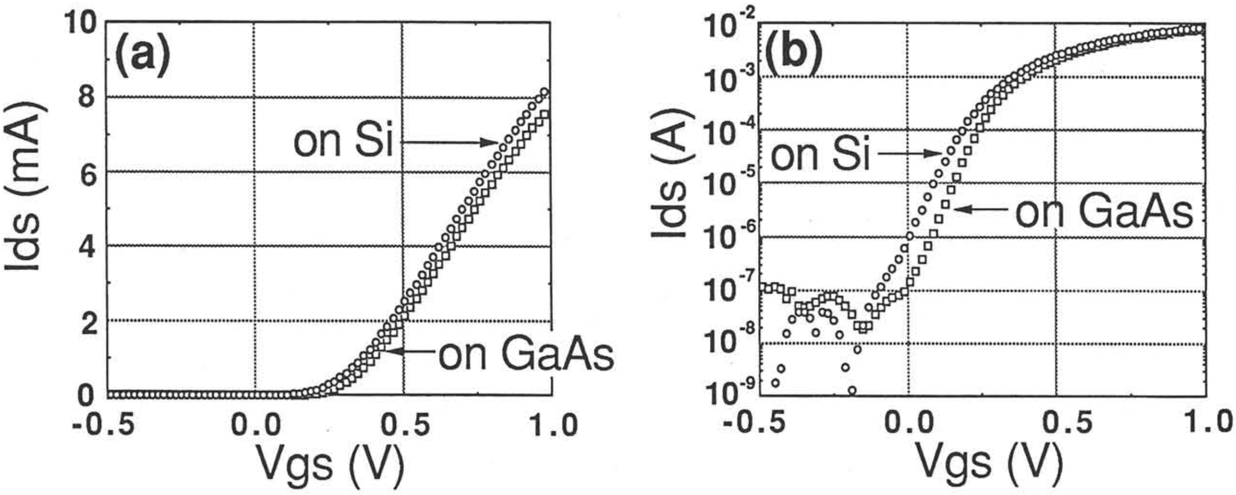

Fig. 2 Drain currents, Ids, of HEMT on Si and on GaAs as a function of gate-to-source voltage, Vgs, with a linear scale (a) and semi-log scale (b). Drain-to-source voltage, Vds, is 1V.

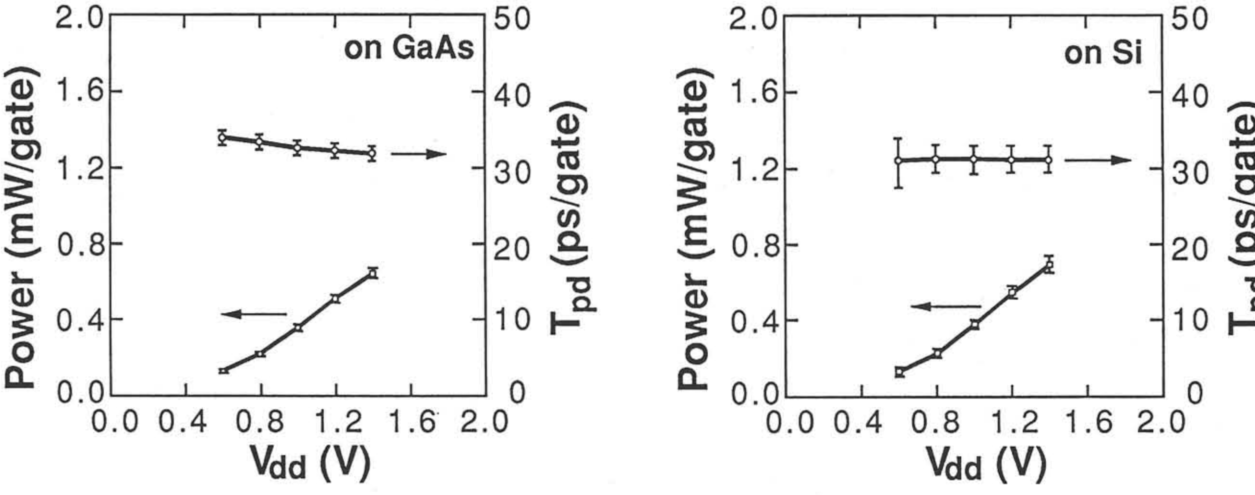

Fig. 3 Basic propagation delay and power consumption per gate of 0.6 μm gate HEMT DCFL circuits as a function of supply voltage. The load HEMT is 5 μm wide and the driver HEMT is 10 μm wide. Error bars show standard deviation.

with a semi-insulating GaAs substrate. These swings do not change much when Vds is smaller. For Vds = 0.3V, swing with Si is 82.5 mS/decade and with GaAs is 75.2 mS/decade. In regions where Vgs is lower than it is in the subthreshold region, Ids is similar with Si and with GaAs. This implies that currents on the GaAs/Si substrate interface and in the GaAs buffer layer are sufficiently suppressed in our GaAs on Si substrates.

DCFL circuit ring oscillators on 3 inch Si substrates had a mean propagation delay of 31.3 ps and power consumption of 0.38 mW/gate with a 1V supply. These values are almost equal to the 32.6 ps delay and 0.36 mW/gate power consumption with GaAs substrates. Recently, with the development of ULSI, supply-voltage scaling has become important for low power operation. We measured propagation delay and power consumption per gate as a function of supply voltage for 0.6 μm gate HEMTs both on Si and on GaAs substrates (fig. 3). The gate width of the load HEMTs were 5 μm, and of the driver HEMTs were 10 μm. Both HEMTs on Si and GaAs substrates can still be high-speed with supply voltage scaled down to 0.6V. The power-delay product is 4.3 fJ for HEMTs on Si substrates with a supply voltage of 0.6V. Subfemtojoule operation will be possible for sub-half micron HEMT ICs on large area operation.

4. CONCLUSION

We demonstrated that InGaP-based HEMTs on Si substrates can make possible high-speed and low power ULSI devices. HEMTs will enable us to make the sub-half micron gate ULSI a reality.

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