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TEM and PL Characterization of GaAs and ZnSe/ZnCdSe Grown on Si

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Two types of GaAs-on-Si structures were studied. The first is ALE-grown GaAs on planar (100) Si substrates and the second is GaAs grown by the two step method on patterned Si. Additionally, ZnSe/ZnCdSe structures were grown on GaAs-coated Si. The structural and luminescent properties of these samples were investigated by transmission electron microscopy and photoluminescence.

1. INTRODUCTION

The development of III-V semiconductors grown on Si substrates has been the subject of intensive research over the last ten years. However, two main problems continue to be major obstacles in the way of further developing these structures. These are the large crystallographic mismatch that results in the formation of a high density of dislocations, and the large thermal expansion mismatch that results in the formation of cracks. Several approaches have been experimented with recently to alleviate these problems. These fall into to general categories. The first involves the improvement of the initial stages of growth. This includes the use of: AlAs to improve the initial nucleation, Si_xGe_{1-x} to gradually accommodate the misfit, II-VI type buffer layer such as ZnSe and using growth techniques that give rise to more two dimensional growth such as ALE, MEE and ion-assisted deposition. The second category involves the improvement of the III-V layer at a stage later than the initial nucleation and growth. This includes using thermal cycle growth and the use of strain layer superlattices. Additionally, selective area epitaxy and the growth on patterned substrates [1] were explored to the same end.

2. EXPERIMENTAL

In this work, two types of GaAs-on-Si structures were studied. The first consists of a thin, ALE-grown GaAs or AlAs on planar (100) Si substrate followed by a thicker, thermal cycle grown (TCG) GaAs layer. The second structure was grown on sawtooth-patterned Si substrates using a two-step deposition process. In both cases the growth was carried out by low pressure MOCVD at Spire Corporation [1]. The ZnSe/ZnCdSe structures were grown by MBE on MOCVD-grown GaAs-on-Si [2]. The motivation for this work is the development of blue emitting lasers and their integration with the Si technology.

The resulting structures were characterized by plan-view and cross-sectional TEM, and photoluminescence (PL). The TEM samples were prepared by mechanical thinning followed by iodine ion beam milling at 4-5 kV. The minority carrier lifetimes were measured by time-resolved PL using pulsed dye-laser excitation and time-correlated photon counting. The 10 ps laser pulses produce PL which is detected with a microchannel plate detector. The system response is approximately 100 ps [3].

3. RESULTS AND DISCUSSION

The nature, density and three-dimensional distribution of defects in the ALE growth were investigated as a function of substrate misorientation, nucleation layer composition and the number of ALE cycles. Planar (100) Si substrates misoriented by either 2° or 4° were used in this study. A TEM cross-section of a structure consisting of ALE GaAs (18 cycles) followed by 1.5μm TCG GaAs, grown on 4° off (100) Si is shown in Fig. 1. Clearly, the majority of the dislocations are confined to the interface region, and are in a misfit configuration. Additionally, the effect of annealing during TCG is evidenced by the formation of closed dislocation loops within 0.5μm from the interface. However, TEM studies showed that growing similar structures on 2° off (100) substrates yield higher density of threading dislocations. High resolution analysis of the GaAs/Si interface region showed a higher proportion of pure edge dislocation in the former than in the latter structures. Pure edge dislocations are more effective in relieving misfit and less likely to generate threading dislocations.

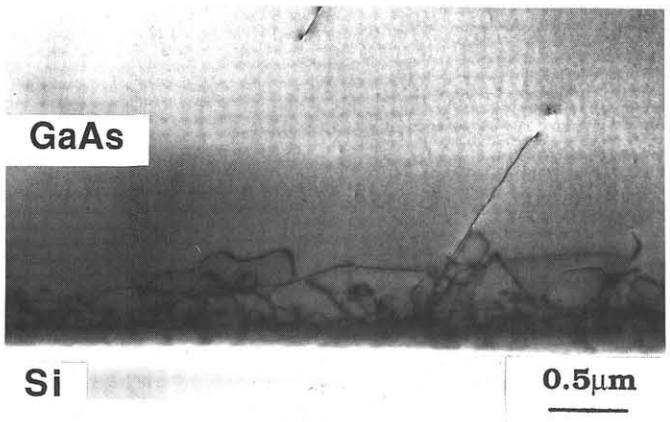

Fig. 1. TEM cross-section of an ALE/TCG grown GaAs on Si.

AlAs was used in this study to replace GaAs in the ALE growth. In general, this gave rise to more two-dimentional growth and better confinement of dislocations to the interface region. This is exemplified in Figure 2 which is a TEM cross-section of a structure consisting of ALE AlAs (18 cycles) followed by 1.5μm TCG GaAs , grown on 4° off (100) Si. Increasing the number of ALE cycles from 18 (which corresponds to a layer thickness of 51 Å) to 71 cycles had no significant effects on the density or distribution of defects.

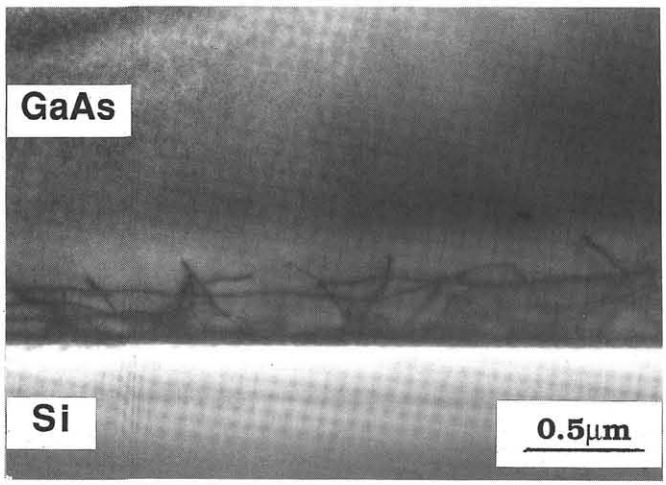

Fig. 2. TEM cross-section of ALE-grown AlAs on Si followed by TCG-grown GaAs.

In order to minimize surface recombination and make meaningful minority carrier lifetime measurements on these structures, an isotype double heterostructure must be fabricated. Therefore, double heterostructure devices with GaAs active regions and GaAlAs confining layers were grown on top of the GaAs-on-Si. The wide bandgap GaAlAs layers serve to reduce the surface recombination velocity of the bare GaAs and to confine the photogenerated carriers within the active layer. It has been shown that for a double heterostructure with an active layer thickness d ($d<\pi^2 D/2S$, where D is the hole diffusivity), the PL decay time τ_{PL} is related to the bulk lifetime τ_B and S by the following equation:

$$\tau_{PL}^{-1} = \tau_B^{-1} + 2S/d. \qquad (1)$$

Note that the PL decay rate is an inverse function of d. The bulk decay rate $1/\tau_b$ is a sum of the radiative and nonradiative recombination rates:

$$\tau_B^{-1} = \tau_{nr}^{-1} + BN \qquad (2)$$

If S is sufficiently small and d is sufficiently large, then: $\tau_{PL}=\tau_B$. Figure 3 shows the PL decay curve of such a DH structure having a well width of 4μm, grown on a structure similar to the one in Figure 1. The measured lifetime is 2.9 ns which is three times higher than that of the best unpassivated GaAs/Si layers. Fitting Eq. 1 to the data indicates that S=1650 cm/s. Similar DH structures grown on bulk GaAs substrates exhibited a lifetime in the 22-34 ns range. The large difference in lifetime between the Si and GaAs based DH structures could be explained by the two orders of magnitude difference in threading dislocation density.

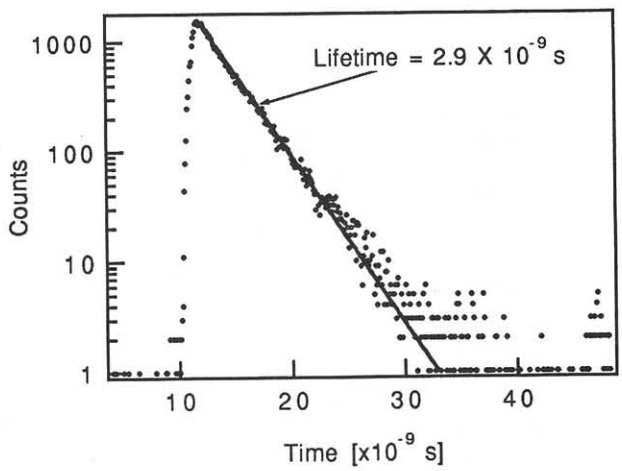

Fig. 3. PL decay curve of a GaAs/GaAlAs DH structure grown on GaAs-on-Si.

TEM cross-sectional examination of GaAs grown on patterned Si showed that most of the samples contain almost perfect saw-tooth shaped GaAs/Si interfaces with the facets on {111} lattice planes. This perfection demonstrates the success of the preparation method which uses a combination of holographic lithography and wet chemical etching. Additionally, TEM revealed a high density of misfit dislocations on the {111} facets of the corrugated substrates. Figure 4 is a weak beam micrograph of such a structure grown by the two-step method without any subsequent heat treatment. Clearly, some threading dislocations propagate from the interface region. The subsequent use of TCG effected a drastic reduction in the density of such dislocations and a better dislocation confinement. The threading dislocation density in these structures varied markedly from one sample to another. One possible factor affecting this is the presence of an amorphous layer at the Si/GaAs interface which was confirmed by High resolution TEM. This layer could be a residual silicon oxide or an incompletely crystallized GaAs layer that is left from the

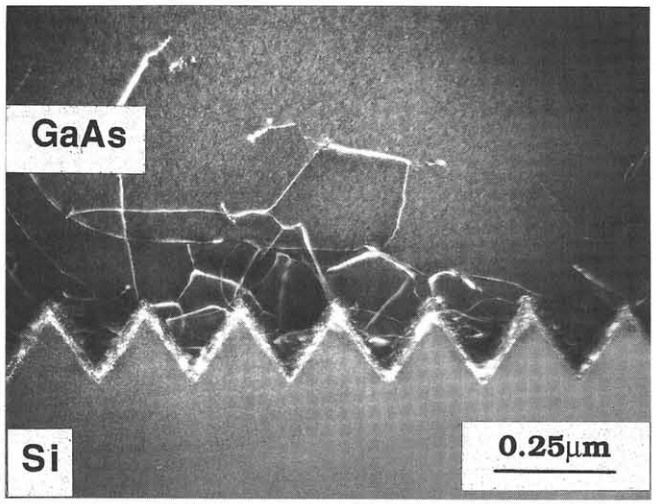

Fig. 4. TEM cross-section of GaAs grown on sawtooth patterned Si.

first step of the two-step growth process. Although many researchers believe that the presence of such an amorphous layer could significantly increase the threading dislocation density, in this particular case it may result in some sort of a seeded epitaxy which could partially alleviate the mismatch problem.

Two different types of ZnSe/ZnCdSe structures were grown. The first consists of: GaAs/750nm ZnSe buffer/100 period ZnSe-ZnCdSe superlattice (SL). The layer thickness in the SL is 8nm for ZnSe and 18nm for ZnCdSe. TEM examination revealed the planar morphology of the superlattice layers (Fig. 5). Additionally, no misfit dislocations were observed in the various interfaces within the SL. However, threading

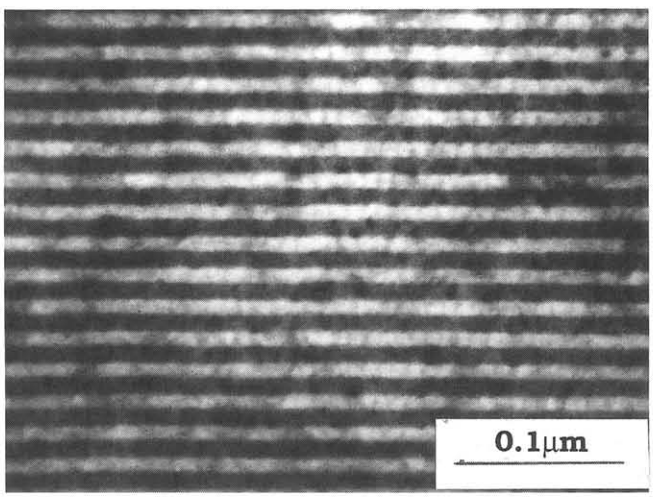

Fig. 5. TEM cross-section of a ZnSe/ ZnCdSe superlattice grown on GaAs-on-Si.

dislocations were observed through the SL. Their density is considerably smaller than that at the top of the GaAs layer. This is believed to be due to the bending of dislocations at the GaAs/ZnSe interface.

The second type of ZnSe/ZnCdSe structures comprises: GaAs/1μm ZnSe buffer/ZnSe-ZnCdSe multiple quantum wells (MQW). Figure 6 shows such a structure having three ZnCdSe wells ranging in thickness

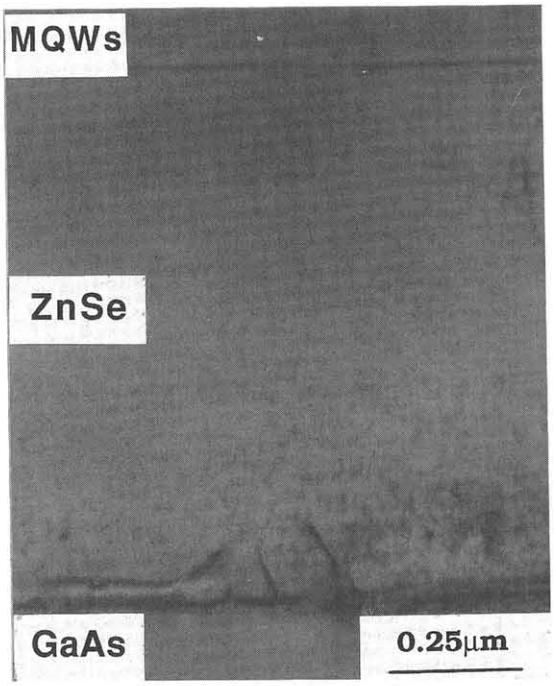

Fig. 6. TEM cross-section of ZnSe buffer /ZnSe-ZnCdSe MQWs grown on GaAs-on-Si.

from 15 to 3nm at the top, with 34nm thick ZnSe barriers. Despite the small (~0.3%) mismatch, a dislocation network is present at the GaAs/ZnSe interface in all samples examined. This is likely due to the relatively high density of threading dislocations in the underlying GaAs layer. It is believed that the small misfit at that interface is enough to bend over a large number of these threading dislocations. The MQW region exhibited defect densities markedly lower than expected. Furthermore, room-temperature and 77K PL spectra indicated a high material quality in this region.

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