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Effect of Dislocation Networks at SLS Interfaces on the Reduction of Threading Dislocations in GaAs/Si

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Dislocation density less than 10^6 cm^{-2} order of magnitude has been realized in GaAs/Si with blocks of strained-layer superlattices(SLSs) having the layers beyond the critical thickness grown by metalorganic chemical vapor deposition(MOCVD). Study of the threading dislocations in these samples indicates that the misfit dislocation network at SLS blocks-GaAs interfaces play important roles in the dislocation reduction.

1. INTRODUCTION

Reduction of threading dislocation is of vital importance in applying GaAs/Si to optoelectronic devices. Many authors have tried to reduce etch-pit density (EPD) to less than 10^6 cm^{-2} by using SLSs within critical thickness in order to prevent the inserted SLSs from generating any dislocations[1],[2]. However, most of the authors were not successful in reducing EPD to below 10^6 cm^{-2} exept for the low temperature growth with the MEE technique[3]. EPD less than 10^6 cm^{-2} has been obtained in GaAs/Si with three blocks of SLSs having the layers beyond the critical thickness. In this paper, reduction mechanism of the threading dislocations in these samples is studied about the following three points:

(1)Bending effect of threading dislocations by misfit strain without no misfit dislocation networks

(2)Sinking effect of threading dislocations into SLS interfaces(interaction between misfit dislocation networks and threading dislocations)

(3)Stress reduction effect on the top GaAs layer

2. EXPERIMENT

The epi-layers studied here were grown by low pressure MOCVD using trimethylgallium,trimethylindium and arsine on 3 inch ϕ (001) Si substrates 3° off toward $\langle 011 \rangle$. The epi-layer structures of sample A and B used are illustrated in Fig. 1, where A has three equivalent $In_xGa_{1-x}As/GaAs$ (x=0.1) SLS blocks (b) and the total epi-layer thickness of 5.2μm, and the InGaAs layer beyond critical thickness was intentionally grown and B has the same structure as A except for the top InGaAs layer of each SLS block as shown in (c). Sample B was grown for the purpose of having less misfit dislocation density at the top of SLS block than in sample A. Both of them were provided with thermal cycle annealing (TCA).

For the investigation of the mechanism

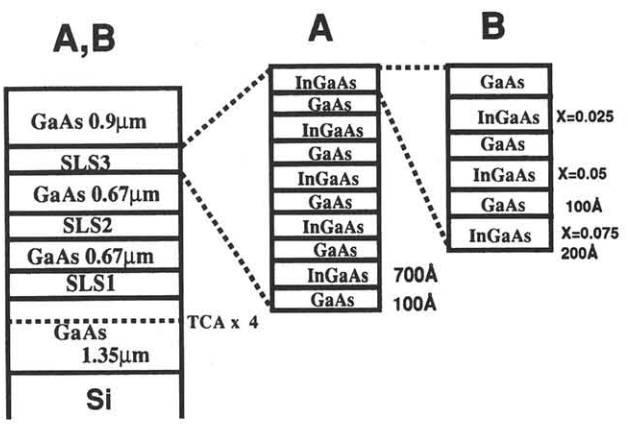

Fig. 1 Sample structure.

of EPD reduction, microscopic observation of the dislocations has been carried out with conventional cross-sectional transmission electron microscopy (XTEM) and an inclined XTEM technique (see Fig. 2(a)) which can obtain combination information of plan-view TEM and conventional XTEM. Macroscopic observation of the threading dislocations was made with depth-profile of EPD. Etching was carried out with molten KOH for EPD and mixture of hydrogen peroxide , hydrofluoric acid and water for layer removal. Residual stress of the sample wafers at the top of GaAs layer was estimated from the difference in X-ray diffraction peaks between the GaAs epi-layer and the substrate Si.

3. RESULTS AND DISCUSSION

EPDs of sample A and B are $4\sim5 \times 10^5$ cm^{-2} and $1.6\sim2.0 \times 10^6$ cm^{-2}, respectively. From X-ray experiment, residual stress of sample A which is crack-free even with the thickness of 5.2μm is found to be 1.5×10^9 dyn/cm^2. It is as large as that of 4μm thick GaAs/Si without SLSs, which suggests that the dislocation networks absorbed the stress taking place in the cooling stage of the growth process.

A XTEM image of SLS1 in sample A is shown in Fig. 3, where it suggests that the threading dislocations are bent at InGaAs-GaAs interface in the SLS blocks, but the effect is not strong enough to stop their climbing up to the upper SLS-GaAs interface. The inclined XTEM was observed in order to investigate the behavior of the threading dislocation at the interface. One of the image of the sample A is shown in Fig. 2(b), where most of the threading dislocations probably originating from the GaAs-Si interface are connected to the misfit dislocation network at the lower SLS-GaAs interface. Most part of the dislocations threading through and/or generating from the lower interface are bent at InGaAs-GaAs interfaces and then sink into the networks of the upper SLS-GaAs interface as is observed in Fig. 2(b).

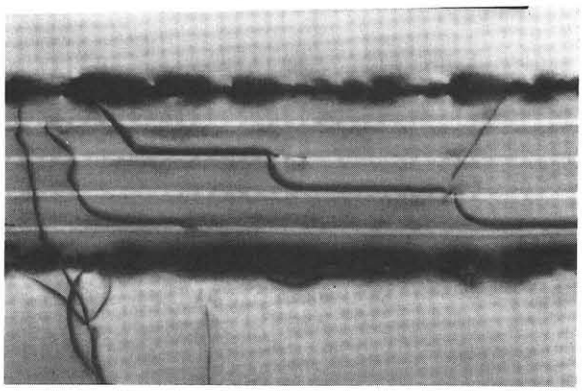

Fig. 3. Conventional XTEM image of sample A

A XTEM image of sample B is shown in Fig.4, where less dense dislocation networks seem to be observed at the upmost SLS block-GaAs interface probably due to the layer structure shown in Fig. 1.

The depth-profile of EPD is shown in Fig. 5, where the horizontal axis indicates the distance from the GaAs-Si interface. Though EPD of both samples is nearly the same in GaAs layer between SLS1 and SLS2 in Fig. 1, EPD of sample A decreases dramatically as compared with that of sample B

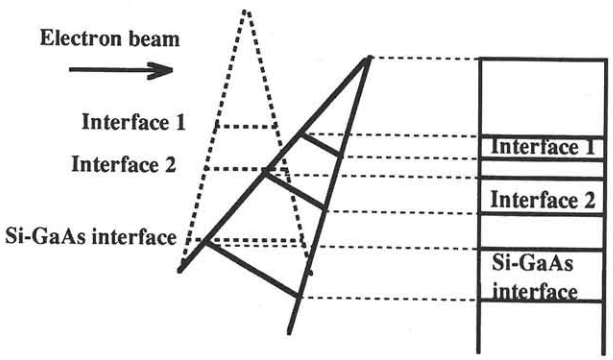

Fig. 2(a) Inclined XTEM shown schematically.

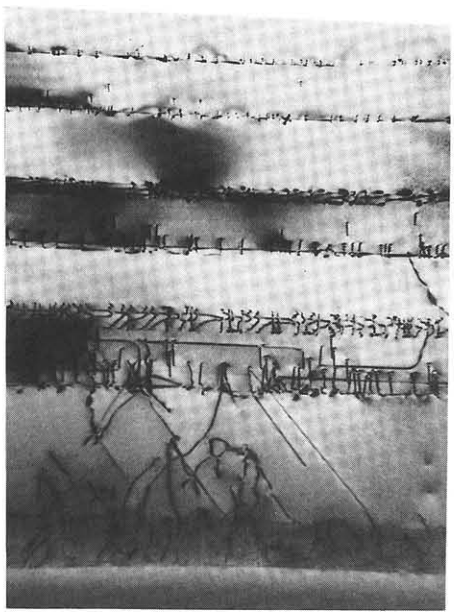

Fig. 2(b) Inclined XTEM image of sample A.

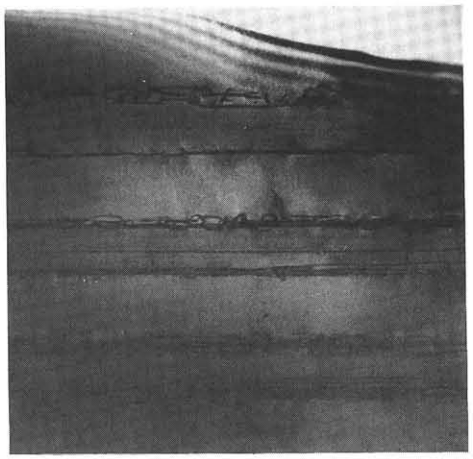

Fig.4 XTEM image of sample B

in the surface GaAs layer. This fact supports that the dislocation network works as a sink of the threading dislocations, when the result of the TEM observations and the depth-profile of EPD are taken into account. This indicates that interaction between threading dislocations and misfit dislocation networks at the SLS-GaAs interfaces works effectively to reduce the threading dislocations. The bending effect of misfit strain is not strong enough to reduce EPD to 10^5 cm^{-2} order of magnitude.

The pure edge and 60°mixed dislocations are well-known in GaAs crystal[4], and it has been reported that misfit dislocations are generated at the multilayer interfaces. Those two type dislocations may interact each other as follows[5]:

$$a/2[10\bar{1}] + a/2[011] \rightarrow a/2[110]. \quad (1)$$

$$a/2[0\bar{1}1] + a/2[110] \rightarrow a/2[101]. \quad (2)$$

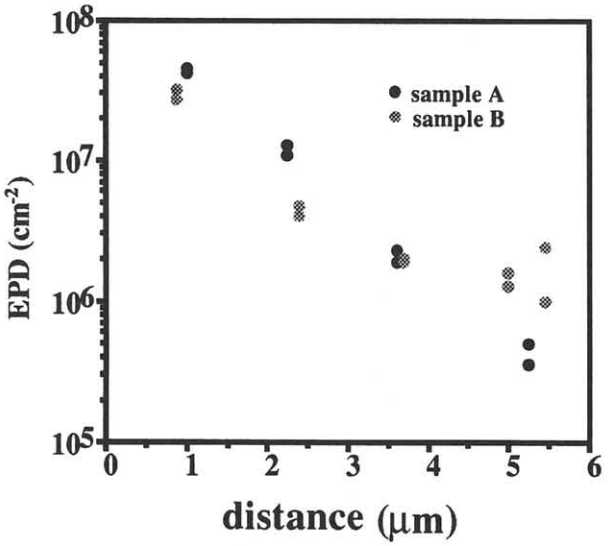

Fig. 5 The depth-profile of EPD of sample A and B

In these formula, (1) indicates that the pure edge dislocations occur and join in the network at the SLS-GaAs interface by the interaction of two 60° mixed dislocations. This interaction works so as to reduce the threading dislocations in GaAs epitaxial layers. These pure edge dislocation with Burgers vectors in the (001) plane may drive to the edge of wafer.

In this experiment, The sample with EPD of 10^5 cm^{-2} order of magnitude has a lot of misfit dislocations at SLS interfaces, and has high probability of interaction between such 60° mixed dislocations and the misfit dislocation networks. However, it is noted that it did not give better results of EPD to increase the alloy composition x in $In_xGa_{1-x}As$ and therefore, to increase the misfit dislocation density at the interface. For example, EPD was found to be $1\sim2\times10^7$ cm^{-2} when x=0.2.

Further studies are nessesary to get optimum condition for the misfit dislocation networks.

4. CONCLUSION

The dislocation networks produced by the SLS blocks with the InGaAs layer more than critical thickness are effective in reducing the density of the threading dislocation in GaAs/Si.

5. REFERENCES

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