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Invited

Initial Growth Stages and Defect Control in GaAs on Si

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Two approaches to suppress threading dislocation generation in GaAs on Si are discussed. First, we briefly discuss an alteration of the growth mode of GaAs films from three dimensional (3D) to 2D by surfactants on Si substrates. Then, the effect of thin Si interlayers on threading dislocation motion in GaAs films is described.

1. INTRODUCTION

Over the past few decades, the formation of misfit dislocations at lattice-mismatched semiconductor hetero-interfaces has been a fundamental concern of continued interest. These dislocations interact with one another at the interfaces and propagate into epitaxial films during the growth and subsequent cooling down of the above materials. The threading parts of these dislocations in epitaxial layers cause serious problems when such materials are applied for device fabrication, since they induce a critical effect on device quality.

In this paper, we report on two approaches to suppress the generation of threading dislocations in GaAs on Si, which we are now developing. First, we briefly discuss an alteration of the growth mode of GaAs films from three dimensional (3D) to 2D by the deliberate introduction of surfactants on Si substrates. Then, we describe the effect of thin Si insertion layers on threading dislocation motion in GaAs films.

2. CONTROL OF INITIAL GROWTH STAGES

A 2D layer-by-layer growth is desired for heteroepitaxial growth to obtain high quality growing films. The perfect termination of dangling bonds on a substrate material by using so-called surfactants[1] is considered to be one of the fundamental requirements for achieving this. We have been applying this process for GaAs on Si in two different ways. One is to passivate the Si (100) surface with 1 ML of S prior to GaAs growth. This S passivation was carried out at a substrate temperature of 300 °C by using an electrochemical Knudsen cell in a multichamber MBE system. Then, GaAs layers were grown on S-passivated Si substrates at a rate of 1 ML/s at 500 °C. All of the growth processes were monitored by carrying out in situ RHEED observations. Figure 1 compares cross-sectional TEM (XTEM) micrographs of 10 nm thick GaAs on Si (a) with and (b) without S passivation. Compared to a direct growth of GaAs on Si, a GaAs layer on a passivated Si surface is close to that under the 2D growth mode, although island growth is not fully inhibited.

Another way is to first grow a layered material of GaSe on an As-terminated Si (111) surface by van der Waals epitaxy.[2] Then, GaAs growth is performed on the above material. Details will be reported at this conference.[3]

3. CONTROL OF THREADING DISLOCATION PROPAGATION

The threading dislocations generated in GaAs on

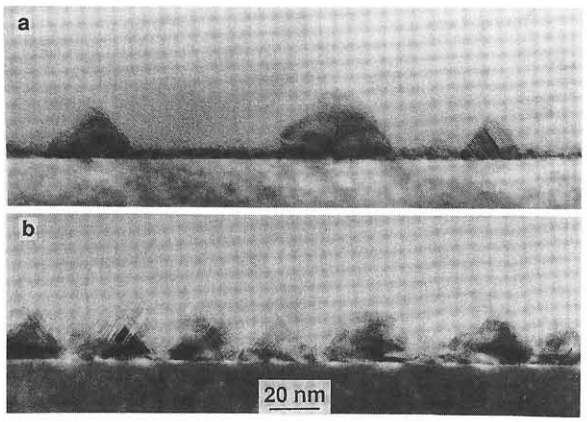

Fig.1 XTEM micrographs showing 10 nm thick GaAs on Si (a) with and (b) without S passivation.

Si change their moving directions at the insertion region of very thin Si interlayers.[4] This is due to a filtering effect of the Si interlayers for dislocation propagation in GaAs caused by the strong covalent bonding of Si-Si. We now discuss this effect.

3.1 Effect of thin Si interlayers

Generally, the running directions of dislocations in GaAs films are effectively influenced by thin insertion layers, such as a strained-layer superlattice. This might result from two different effects, as shown in Fig. 2. One effect is a blocking effect (Fig. 2 (a)) which is due to the different hardness between the growing film and the inserted material. For example, the shear modules, μ, of GaAs and Si is 3.29×10^{11} dyn/cm^2 and 6.45×10^{11} dyn/cm^2, respectively. Another effect is a sweeping out effect (Fig. 2 (b)), which is mainly induced from the misfit strain between the film and the inserted layer. The induced stress is proportional to the product of (μfdh), where f is the misfit between the film and interlayer, b is the magnitude of the Burgers vector of the dislocation, and h is the interlayer thickness. In the case of using Si as an insertion layer, the maximum thickness is ~1 nm for the generation of no defects in the inserted GaAs films.[4]

Figure 3 shows a schematic cross-section of the sample structures used for experiments involving

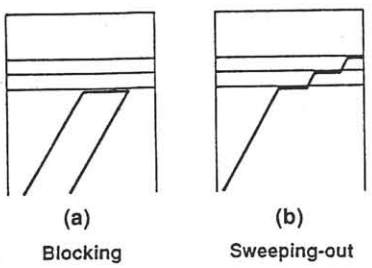

Fig.2 Effect of insertion layers on dislocation movement in heteroepitaxial films.

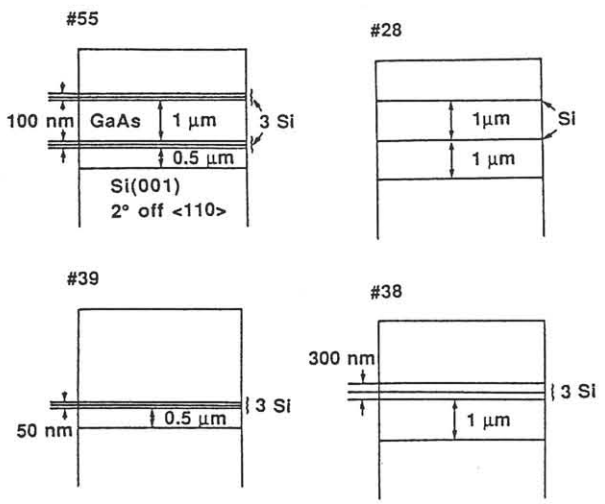

Fig.3 Schematic cross-section of sample structures used for experiments.

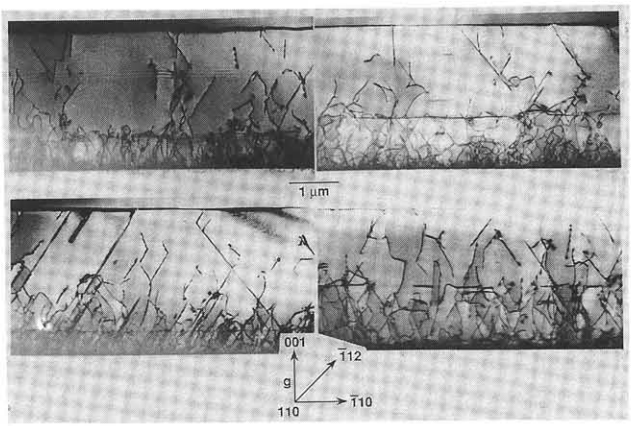

Fig.4 XTEM micrographs showing threading dislocation morphologies in different samples corresponding to Fig.3. Sample 55, 28, 39 and 38 are from upper left to lower right, respectively.

threading dislocation observations. In each sample, the inserted Si thickness was 1 nm (details concerning the sample preparation conditions are described elsewhere)[4]. Figure 4 compares the threading dislocation morphologies in different samples corresponding to the sample structures shown in Fig. 3. We can clearly see that some dislocations running along the <110> and <211> directions on the {111} planes inclined from the (100) substrate change their running directions by the effect of Fig. 2 into the $\pm[\bar{1}10]$ directions parallel to the interface at the Si insertion positions. The nature of the threading dislocations passing through thin Si regions was evaluated in separate dislocation contrast experiments. The dislocations having difficulty to change their moving directions were mainly 30°-type dislocations along the <211> direction and screw-type dislocations running parallel to the [001] growth direction.

3.2 Combined effect of Si interlayers and annealing

In order to further reduce the dislocation densities which reach the sample surface by threading over the Si barriers, we carried out annealing of the samples after growth under the different conditions (mainly at 800 and 900 °C for 10 s, and at 800 °C for 30 min). Annealing as a thermal process activates the dislocation slip systems. Therefore, we could therefore expect that combining Si insertion with annealing would enhance the interaction of the threading dislocations with the strained interfaces, as typically shown as 4 features for sample 28 in Fig. 5, resulting in a dislocation density reduction at the top surface. In this case, the sweeping out effect in Fig. 2 (b) mainly acts to bend the dislocations.

Figure 6 shows the threading dislocation morphologies annealed at 900 °C for 10 s for samples corresponding to Fig. 3. Compared to dislocation morphologies observed in Fig. 4, the long, straight dislocations along the <211> direction seen in all of the samples in Fig 4 disappeared after annealing. We also note that the number of dislocations which were bent toward the $\pm[\bar{1}10]$ directions at the Si insertion positions increased in Fig. 6. Particularly, this feature is remarkably observed for sample 55, indicating that the gliding phenomenon of dislocations was enhanced by annealing, for example, according to Fig. 5 (d). However, there still exists an appreciable number of dislocations which thread into the overlayer passing through the interlayers. This suggests that the layers of Si are too thin to fully block the gliding dislocations. It is thus necessary to use other materials which could enable us to introduce thicker layers into GaAs, sufficient to block the dislocations.

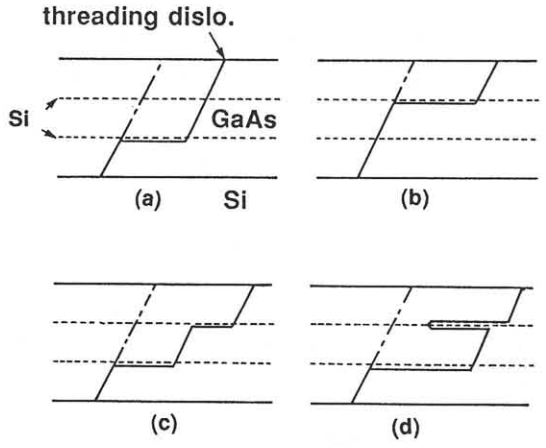

Fig.5 Schematic representation showing threading dislocation movements in sample 28 during annealing.

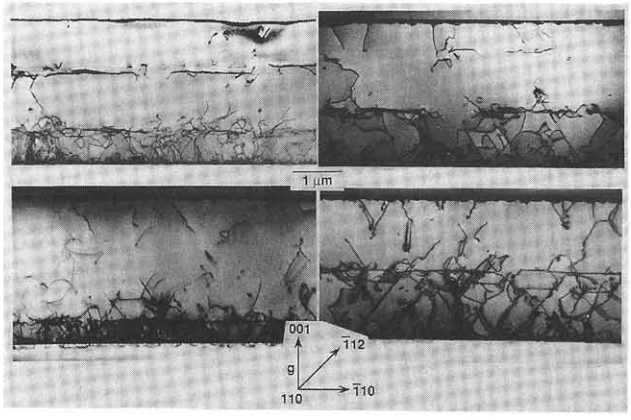

Fig.6 XTEM micrographs showing threading dislocation morphologies annealed at 900°C for 10s for samples corresponding to Fig.3. Sample 55, 28, 39 and 38 are from upper left to lower right, respectively.

3.3 Application for other systems

We applied GaAs layers having thin Si layers on Si substrates for subsequent InP growth. The use of GaAs buffer layers helped us to improve the structural properties of InP grown on Si. Since they provide an intermediate lattice constant between those of InP and Si. A typical example of XTEM micrographs is shown in Fig. 7 for this growth. InP growth was carried out in a low pressure MOCVD reactor at 600 °C just after completion of the GaAs growth on Si substrates.[5] In this case, $In_{1-x}Ga_xP$ interlayers are also placed at different compositions and depths in InP as shown in the figure. The threading dislocation density in InP ranges about mid to high $10^7/cm^2$ in the neighborhood of the top surface. This value is comparable to that obtained for InP layers grown directly on GaAs substrates[6], and to the reported ones after annealing in InP/GaAs/Si structures.[7] On the other hand, it is one order of magnitude smaller than those for InP layers grown directly on Si.[7]

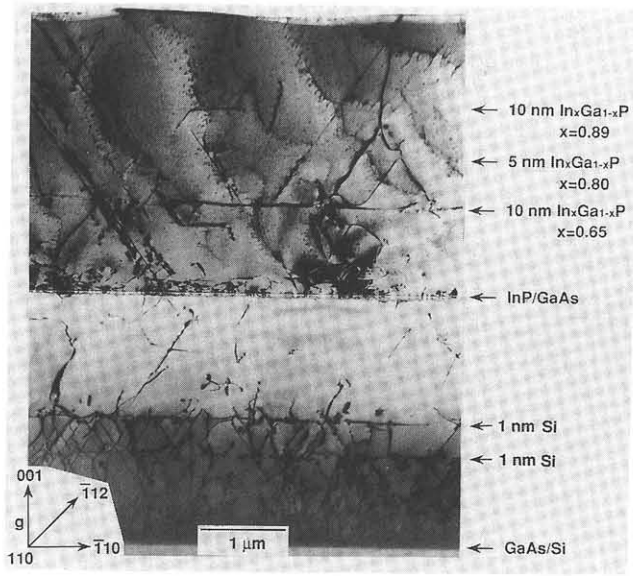

Fig.7 XTEM micrograph showing dislocation morphology in InP/GaAs/Si.

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