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A New Single Electron Transistor

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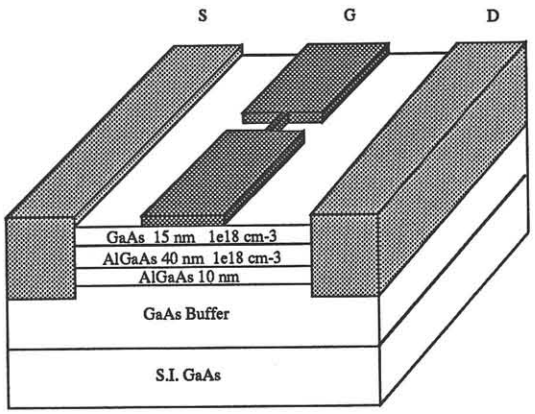
We propose and demonstrate a new single electron transistor with a nanoscale single barrier placed inside the gap of a conventional split-gate FET. At low temperatures, as the gate voltage was scanned, reproducible periodic oscillations of drain conductance were observed before the onset of the first $2e^2/h$ conductance plateau. The shape of the oscillation peak can be well fitted by the derivative of the Fermi-Dirac distribution. It was found experimentally that each conductance oscillation corresponds to the Coulomb blockade of a single electron in the one-dimensional channel. A model that describes the operation of the new single electron transistor is suggested.

1. INTRODUCTION

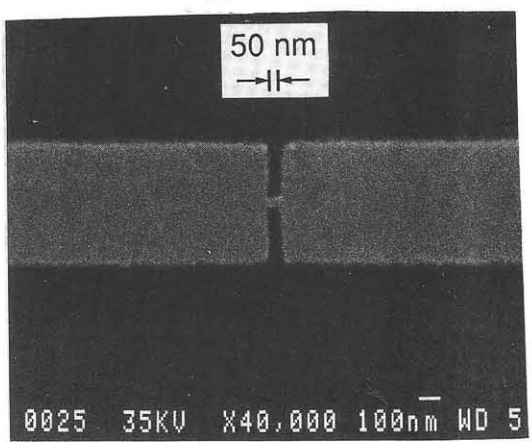
As the size of semiconductor devices continues to shrink, their capacitance may decrease to a point where the effects of single electron charging significantly affect device operation. Such Coulomb effects are not only interesting in physics, but also open up new possibilities for new electronic devices. Previously, in semiconductor devices, single electron Coulomb blockade in a field-effect transistor (FET) that has a quantum well confined between two barriers was reported.[1] The double barrier scheme was believed to be critical to retain a single electron. Here, we present the first experimental study of a nanometer FET with a *single* barrier in its one-dimensional channel and suggest a model for its operation. We report observing, in addition to $2e^2/h$ conductance plateaus, reproducible periodic conductance oscillations before the onset of the first $2e^2/h$ plateau, and we show that these oscillations are due to the Coulomb blockade of a single electron.

2. FABRICATION AND MEASUREMENT

The single-barrier nanometer FET has a structure similar to a split-gate FET, except that a metal barrier is placed in the middle of the gate gap (Fig. 1a). Using a negative gate bias, the electrons underneath the gate will be depleted, creating two one-dimensional (1D) channels separated by a single potential barrier. The gate was fabricated using ultra-high resolution electron beam lithography and a lift-off process.[2] The width of the metal



(a)



(b)

Fig. 1 (a) Schematic and (b) scanning electron micrograph of a nanometer FET with a single barrier.

barrier and the gap between the two constricted gates as small as 50 nm were fabricated (Fig. 1b). The single-barrier FET (SBFET) has a heterostructure, grown by MBE, consisting of a 500 nm thick layer of undoped GaAs on top of a semi-insulating GaAs substrate, followed by a 10 nm undoped $Al_{0.3}Ga_{0.7}As$ spacer layer, a 40 nm $Al_{0.3}Ga_{0.7}As$ layer doped with a Si concentration of $1x10^{18}$ cm^{-3}, and a 15 nm GaAs cap layer with a Si doping concentration of $1.4x10^{18}$ cm^{-3}. The two-dimensional electron gas (2DEG) formed at the GaAs/AlGaAs interface had a Hall mobility of 12 m^2/Vs and a carrier concentration of $8.9x10^{11}$ cm^{-2} at 77 K in the dark. For comparison, constricted-gate FETs without any barriers were also fabricated on the same substrate.

The devices were cooled to 0.5 K using a sorption-pumped ^3He refrigerator. Before cooling to 0.5 K, the devices were illuminated by a light-emitting diode (LED) at 10 K and were found to hold a constant 2DEG concentration at 0.5 K for hours. As the gate voltage was scanned, the SBFET with a 50 nm gate gap and a 50 nm wide metal bar showed nine repeatable periodic oscillation peaks in the drain current, in addition to $2e^2/h$ conductance plateaus, before the onset of the first $2e^2/h$ conductance plateau. The oscillation period was 15 mV. The SBFET with a 100 nm gate gap and a 50 nm wide metal bar showed five repeatable periodic oscillation peaks in the drain current with a periodicity of 9 mV before the onset of the first $2e^2/h$ conductance plateau (Fig. 2). Such periodic conductance oscillation peaks were absent when the conductance of the devices was greater than $2e^2/h$. They were also absent in the devices that were fabricated on the same substrate but had a straight constricted gate of the same size without any barrier.

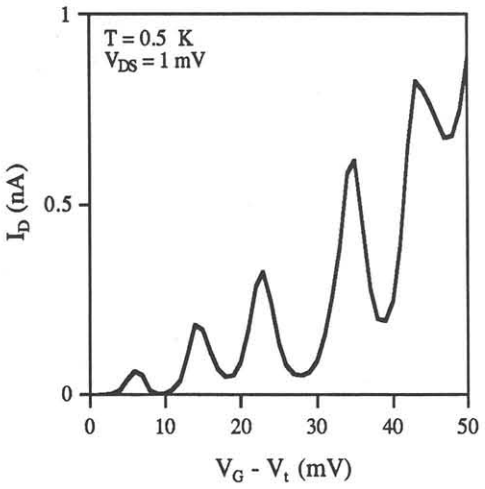


Fig. 2 The drain current vs. the gate voltage before the onset of the first $2e^2/h$ conductance plateau.

The periodic oscillations were very reproducible and the oscillation period remained constant under thermal cyclings, photon excitations, and reversion of the source-drain current. We thermally cycled the 50 nm gate gap device seven times and the 100 nm gate gap device two times from 0.5 K to 300 K, and found that the oscillation period did not change. We illuminated the devices at 0.3 K using a light-emitting diode, and found that the only change was a shift of the entire I-V curve toward the negative gate voltage by a few tenths of a volt; there was no change in the oscillation period. Finally, we exchanged the source and the drain and found that the oscillation amplitude varied slightly, but again there was no change in the oscillation period. These observations indicate the oscillations are not due to impurities.

3. DATA ANALYSIS

To find the physical origin of the conductance oscillations, we first used experimental data to find the gate voltage needed to place a single electron into one of the two 1D channels. The total number of electrons placed in one 1D channel at the 1D-to-2D transition point in the drain current vs. the gate voltage curve can be determined from the conductance and the channel width at the transition point.[3] The channel width at the transition point is approximately the gate gap defined by lithography.[4] Dividing the gate-voltage difference between the turn-on point and the transition point by the total number of electrons at the transition point gives the gate voltage needed to put a single electron into the 1D channel. Thus, we found that the gate voltage needed for placing a single electron into one 1D channel is about 14.6 mV for the SBFET with the 50 nm gate gap and 9.7 mV for the 100 nm gate gap. This agrees well with the experimentally observed current oscillation periods, 15 mV and 9 mV, indicating that the oscillation originates from Coulomb blockade of a single electron. We should emphasize that the determination of the gate voltage needed for a single electron charging is based completely on experimental data and that no fitting parameter is involved.

Secondly, we found that each oscillation peak fits well with the derivative of Fermi-Dirac distribution function (Fig. 3). This means that the width of the current oscillation peak is due to the thermal broadening of a discrete energy level, since the conductance at finite temperature will be the convolution of the conductance at zero temperature and the derivative of Fermi-Dirac distribution function.

Thirdly, the periodic oscillations in the SBFET were seen only when the conductance was less than $2e^2/h$ (i.e., before the onset of the first $2e^2/h$ conductance plateau). According to the single-electron Coulomb

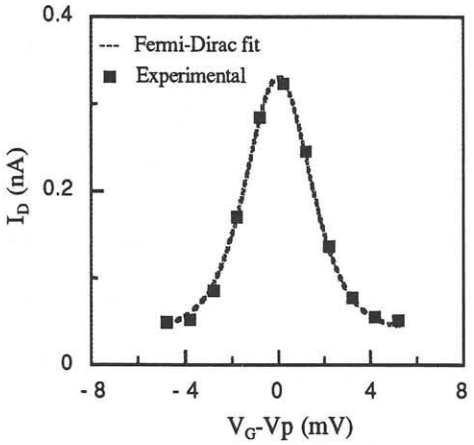


Fig. 3 Fitting by the derivative of Fermi-Dirac distribution. Peak gate voltage offset to zero.

blockade theory,[5] in order to observe the Coulomb blockade effects, a single electron has to remain in a Coulomb state long enough to make energy uncertainty less than the spacing between the two adjacent Coulomb levels. This requires the conductance of the device be less than $2e^2/h$, which is consistent with our experimental observation.

4. PROPOSED MODEL

From the above data analysis, we now suggest a model that describes the operation of the single barrier FETs. The electrons put into the 1D channel will occupy the discrete Coulomb energy levels, while the 2DEG outside the 1D channel have a constant Fermi level. As the gate voltage is changed, the Coulomb levels in the 1D channel are shifted either up or down relative to the Fermi level of the 2DEG. The current peaks when a Coulomb level is aligned up with the Fermi level, and drops when the Fermi level is between the two Coulomb levels. Therefore, the conductance oscillates as the gate voltage moves the Coulomb energy levels in the 1D channel across the Fermi level.

In all previous single electron charging experiments, two or more barriers were used to retain a single electron. In our devices, although there is only a single barrier in the channel, we believe that a single electron can still be retained in the 1D channel at the source side for a period of time. This is because at one end of the 1D channel, the source-drain electrical field pushes electrons back to the 1D channel, and at the other end, the single barrier blocks the electron from entering the drain. From energy band diagram point of view, the electric field between the source and drain tilts the energy band, so that the tilted energy band and the single barrier form a triangle potential well, which retains electrons in a similar way as a potential well created by double barriers.

5. CONCLUSION

In conclusion, we have experimentally studied a nanometer single barrier FET. We observed reproducible periodic conductance oscillations before the onset of the first $2e^2/h$ conductance plateau. The oscillation periods were 15 mV and 9 mV for devices with 50 nm and 100 nm gate gaps, respectively. It has been shown that the oscillation is due to Coulomb blockade of a single electron. This is the first observation of Coulomb blockade of a single electron in a transistor that has only one barrier. A model for the device operation is proposed.

6. ACKNOWLEDGMENTS

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