Extended Abstracts of the 1992 International Conference on Solid State Devices and Materials, Tsukuba, 1992, pp. 741-743

A Single Transistor Static Memory Cell: Circuit Application of a New Quantum Transistor

C.H. Yang, J. Chen, R.A. Wilson and C.E.C. Wood

Joint Program for Advanced Electronic Materials and
Electrical Engineering Department, University of
Maryland, College Park, MD 20742, U.S.A.

We report our recent experimental realization of a new quantum transistor. The operation of the transistor is based on quantum tunneling, i.e., the resonant tunneling current between two terminals can be controlled by a third terminal. In addition to new transistor characteristics, we have also demonstrated that our quantum transistor can function as a static memory cell, which normally consists of six conventional transistors.

1. TEXT

Transistors based on resonant tunneling (RT) have recently attracted much attention. This in part is because there is a challenge to better understand the physics governing the operation of devices of nanometers in size. Research in this field is also driven by the expectation that circuit complexity might be drastically reduced, resulting from novel characteristics of quantum transistors. The major technical difficulty in fabricating quantum transistors is in contacting a quantum well, which is usually separated from heavily doped contact regions by thin quantum barriers[1]. In spite of the difficulties in processing, quantum transistors, and hot-electron transistors in general, are potentially attractive for high-speed electronics. Based on the theoretical traverse time of hot-electrons in bulk GaAs, operation up to THz has been predicted[2]. Such prediction in fact is supported by a recent observation of 2.5 THz infrared detection by using a double-barrier (DB) RT diode[3], and the observation of subpicosecond base transit time in a hot-electron transistor.

Here we report a new unipolar, three-terminal quantum transistor. In the following, we will describe the transistor structure, characteristics, and a particular application in static memory. A typical structure, grown by molecular beam epitaxy on n^+ doped (100) GaAs substrate, consists of an n^+ GaAs buffer layer ($10^{18}/cm^3$, 5000 Å), an undoped $Al_{0.5}Ga_{0.5}As$ barrier (5000 Å), an n^+ doped GaAs quantum well (QW), ($10^{18}/cm^3$, 150 Å) an undoped DB RT structure (30Å$Al_{0.5}Ga_{0.5}As$ /100ÅGaAs/30Å$Al_{0.5}Ga_{0.5}As$) as an energy-momentum filter, an n^+ doped GaAs cap layer ($10^{18}/cm^3$, 2000 Å), and finally a 400Ågraded $In_xGa_{1-x}As$ layer for non-alloying ohmic contact. The indium concentration is graded from x = 0 at the $In_xGa_{1-x}As$ / GaAs interface to x = 0.4 at the surface. The transistor structure and bonding pads are defined by standard processing techniques, including photolithography, mesa etching, deposition of silicon dioxide, evaporation of metal films, and lift-off. The two symmetric contacts at the top are operated as source and drain, and the substrate (and the buffer layer) as the gate. The recessed region between the source and the drain is wet-etched until there is no conduction between the source and the drain at small drain-source biases, when the gate bias V_{GS} is zero. Due to Fermi level pinning at GaAs surface, although the doped GaAs region near surface is not completely removed, the QW region is already depleted at zero V_{GS} . When V_{GS} is positively biased, a conduction between the source, and the drain is made possible only by a sequential process: (a) tunneling-in at the source; (b) lateral transport; (c) and tunneling-out at the drain. Fig. 1 shows the schematic cross section of our transistor.

Figure 2 (a), (b), and (c) show the drain current (I_{Drain}), source current (I_{Source}), and gate current (I_{Gate}), as a function of drain-source voltage (V_{DS}), under different gate biases (V_{GS}) at 77K, respectively. The source is common. For a small V_{DS} ($0V < V_{DS} < \sim 0.5V$), the conduction between source and drain is simply resistive. However, as V_{DS} is increased, I_{Drain} and I_{Source} display the NDC behavior. In contrast, I_{Gate} is orders of magnitude smaller than I_{Source} and I_{Drain} in a wide range of V_{DS} , and I_{Gate} only becomes significant when I_{Drain} and I_{Source} become smaller.

The characteristics are explained as follows. When V_{GS} is zero, the QW is not conductive for that there are no electrons in the QW. The QW channel is made

conductive only when V_{GS} is positively biased, similar to the case of all enhancement-mode FETs. Near zero V_{DS} , the lateral transport in the QW is the most resistive among the three, so that the I_{Source} and I_{Drain} are linear to V_{DS} . As V_{DS} is increased to $\sim$ 0.5V, the tunnel-out junction breaks up the energy alignment (as shown in the upper-right energy band diagram in Fig. 1) and result in the first NDC. The resonant tunneling process here is similar to what has been extensively studied in DB RT diodes, but now the source electrons are two-dimensional. The peaks in I_{Drain} (and I_{Source}) are originated from the tunneling-out junction from the following two observations. First, a semiconductor sample system will always find a self-consistent solution, and it is the drain side that would share a larger voltage drop because of screening. The theoretically expected band bending at the tunneling-in and tunneling-out junctions are shown in Fig. 1. Second, The I_{Drain} (and I_{Source}) increases as the V_{GS} is more positively biased. A more positively biased gate will increase n_{2D}, and a higher n_{2D} would make tunneling-out current larger. This is based on the independent-electron tunneling model:[4] $J = \int dE|T|^2 e n_{2D}(E) v(E)$, where T is the tunneling probability, $n_{2D}(E)$ is electron concentration, and v is the velocity.

Here we emphasize that although the transistor structure looks similar to a series combination of two DB RT junctions and an FET, the characteristic NDC features cannot be reproduced by simply wiring up[5] two separated DB RT diodes and an FET. The difference is evident in that, as shown in Fig. 2, the amplitudes of the current peaks can be tuned by V_{GS} , but the voltage positions do not shift for different V_{GS} .

The NDC feature shown in Fig. 2 can be applied in circuits, such as a memory cells. Fig. 3(a) shows again the output characteristics of a quantum transistor, and the common source configuration is shown as inset. The load line is determined by the supply voltage V_{DD} and the load resistor is R_L. Fig. 3(b) shows the input and output voltage traces, by which we demonstrate the bistable switching. The load resistor is 823kΩ , and the input impedance of the oscilloscope is 1MΩ . For $V_{GS} = 3.4$V, there are two stable operating points, B and C. When the gate is momentarily pulsed to 3.8V and return to 3.4V, the operating point is shown to be switched to point A and return to point B. As shown in Fig. 3(b), The output voltage at the drain contact would then be kept at 0.8V, irrespective of the fact that the gate voltage is already switched back to 3.4V. By the same token, the quantum transistor can be momentarily switched to operating point D by a 3V gate pulse, and then turns stable around point C with an output voltage of 1.5V. The results shown in Fig. 3(b) are in excellent agreement with DC characteristics shown in Fig. 3(a). A RHET[6] has also been shown to operate as a static memory cell, but it needs a large 'base current' to drive the transistor due to the small current gain.

In summary, we have reported a new transistor based on resonant tunneling. Important for circuit applications, our quantum transistor preserves the characteristic high input-impedance and large voltage-gain and power-gain of FETs. The output characteristics, including the voltage swing and the transconductance, can be fine-tuned for cascading single transistors. The fabrication process of our transistor is simplified by using a 'tunneling-in' and 'tunneling-out' approach, which also makes circuit application more feasible.

This work is supported in part by ONR/DARPA.

2. FIGURES

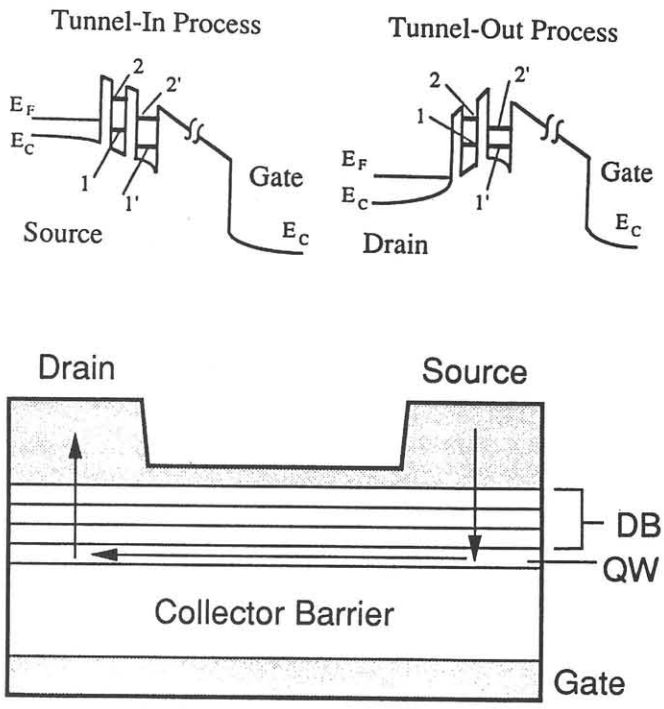

Figure 1: The schematic cross section of of our transistor structure. The energy band diagrams at the 'tunneling-in' and the 'tunneling-out' junctions are also shown, where E_C is the conduction band minimum, E_F is the Fermi level, 1, 2 depicts the lowest two subband levels in the DB RT structures, and 1', 2' depicts the lowest two subband levels in the QW.

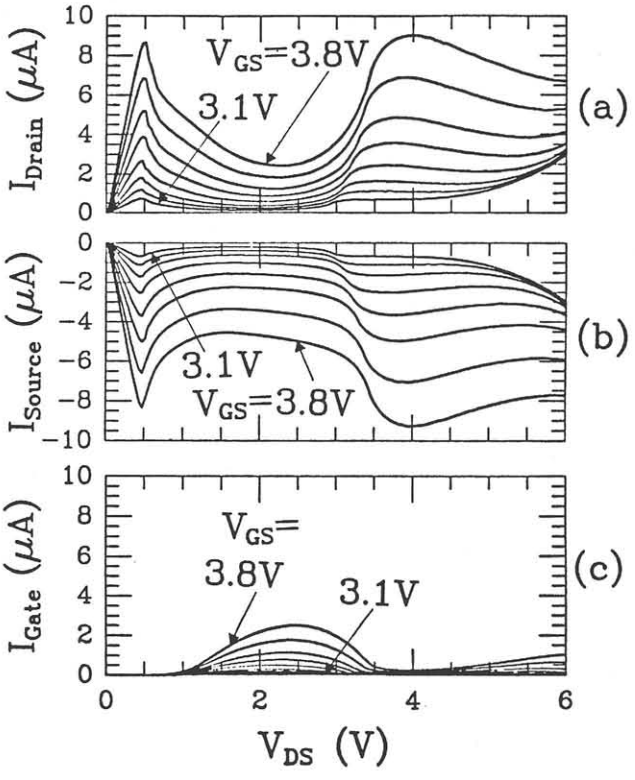

Figure 2: DC I-V characteristics of our transistor at 77K, where (a) I_{Drain} versus V_{DS} , (b) I_{Source} versus V_{DS} , and (c) I_{Gate} versus V_{DS} , are shown. The V_{GS} is stepped evenly from 3.1V to 3.8V.

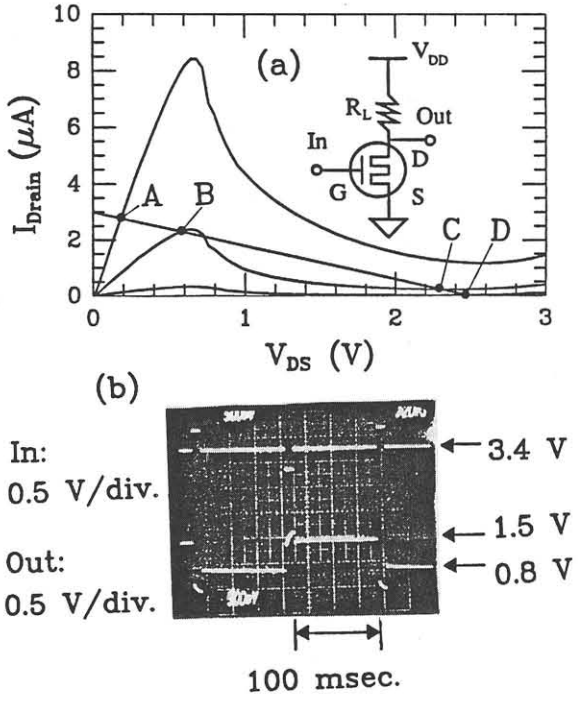

Figure 3: (a) DC I-V characteristics of our transistor at 77K, and the circuit configuration and the load lines are also shown in the inset. The power supply voltage V_{DD} is 2.47V. The operating points discussed in the context are labeled as A, B, C, and D. (b) Waveforms of input (V_{GS}) and output voltage signals.

3. REFERENCES

1. N. Yokoyama, K. Imamura, T. Ohshima, H. Nishi, S. Muto, K. Kondo, and S. Hiyamizu, IEDM Tech. Dig. p. 532 (1984).

2. M. Heiblum, Solid-State Electronics, 24(1981) 343.

3. T. C. L. G. Sollner, W. D. Goodhue, P. E. Tannenwald, C. D. Parker, and D. D. Peck, Appl. Phys. Lett. 43(1983) 588.

4. C.B. Duke, Tunneling in Solids, Solid State Physics Supplement 10, edited by F. Seitz, D. Turnbull, and H. Ehrenreich (Academic Press, New York) 1969.

5. T.K. Woodward, T.C. McGill, H.F. Chung, and R.D. Burnham, Appl. Phys. Lett. 51(1987) 1542.

6. N. Yokoyama and K. Imamura, Electron. Lett. 22(1986) 1228.