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High Speed 0.1 μm CMOS Devices Operating at Room Temperature

A.Toriumi, T.Mizuno, M.Iwase, M.Takahashi, H.Niiyama, M.Fukumoto, S.Inaba, I.Mori and M.Yoshimi

ULSI Research Center, Toshiba Corporation

1, Komukai Toshiba-cho, Kawasaki 210, Japan

Abstract

We report the feasibility study of 0.1μm CMOS devices operating at room temperature, which have been fabricated with the process and device technologies available in the current ULSIs. The significant improvement of DC driving performance and propagation delay time in the ring oscillator provide a direct evidence in favor of further miniaturization of CMOS devices down to 0.1μm for room temperature operation.

1. Introduction

The miniaturization limit of Si-MOSFETs has been recently discussed from the technological as well as the economical viewpoint. We put aside the economical issues in this paper, and will focus on the technological prospect in the future. Recently, several papers have reported on 0.1μm MOSFETs[1]-[2], particularly in terms of low temperature operation. For practical viewpoints, however, the feasibility study of the room temperature operation is strongly needed, where the main problem is the reduction of the threshold voltage to meet the low power supply voltage with maintaining higher short channel effect immunity. Otherwise the higher performance cannot be achieved with scaling down the device size. In this paper, we will describe both high DC performance and fast switching speed in CMOS devices operating at room temperature.

2. Devices

We used the conventional fabrication techniques available in the current ULSI processes. The devices were fabricated on N type (100) wafer with 1~2 Ωcm. The gate oxide was 40 Å grown at 800°C. A 2000 Å thick undoped poly-silicon was deposited and the gate electrode down to 0.09μm was patterned by the electron beam lithography and by the highly selective RIE. Figure 1 shows an SEM picture which shows a 0.10μm patterned gate after the poly-silicon RIE. Special cares were taken to reduce the short channel effects as follows; (1) the LDD with pocket structure for both n- and p-channel MOSFETs, (2) the rapid thermal annealing for 20 sec at 1000°C to activate the implanted impurities, and (3) the surface channel type for p-channel as well as for n-channel MOSFETs, which means the dual gate structures. Furthermore, to minimize the parasitic effects, the self-aligned titanium silicide (salicide)

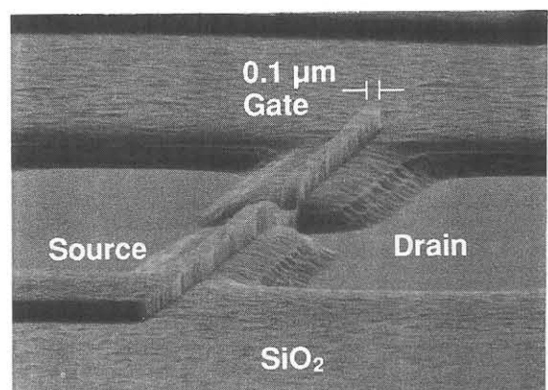

Fig.1 An SEM picture of 0.10 μm gate length MOSFET after the poly-silicon RIE.

technology was employed and the channel implantation was restricted only near the active channel region. The impurity concentration in the substrate, which was measured by the SIMS, was nearly $1\times10^{18}cm^{-3}$ for both n- and p-channel devices at the peak position of 800 Å from the surface, while it was $1\sim3\times10^{17}cm^{-3}$ at the interface.

3. Results and Discussion

We have defined the gate length by the gate polysilicon length, which was measured by the SEM. Figure 2 shows the Id-Vd characteristics for both n- and p-channel 0.10μm MOSFETs, which look quite normal. The gate length dependences of threshold voltage and of subthreshold slope are shown in Fig.3. From these results, we can safely say that the MOSFETs with n-channel down to 0.12μm and with p-channel down to 0.15μm operate very well at room temperature. The measured (not calibrated) transconductances (Gm) are 450 mS/mm for n-channel and 260 mS/mm for p-channel MOSFETs, respectively. We have focused on the gate length dependence of the inverse of transconductance as shown in Fig.4, where the steeper increase of Gm

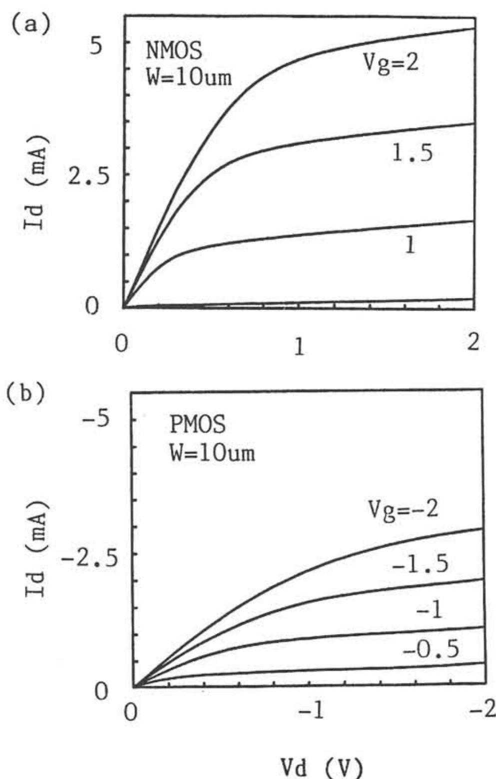

Fig.2 Id-Vd characteristics of 0.10μm (a) n-channel MOSFET, and (b) p-channel MOSFET, respectively.

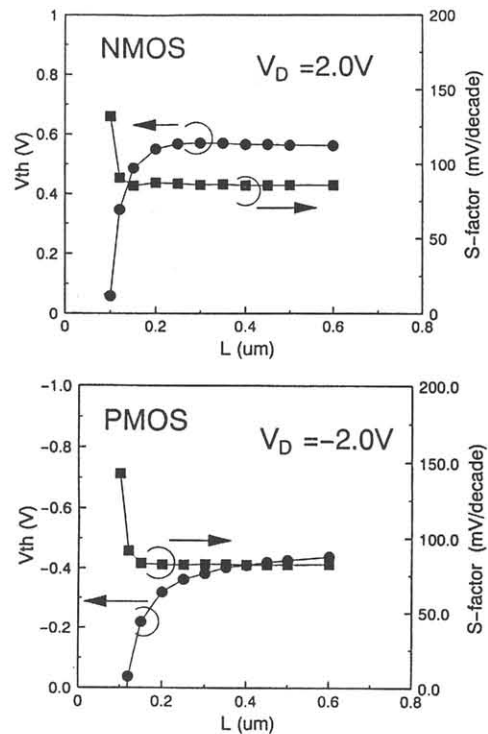

Fig.3 The gate length dependences of threshold voltage and subthreshold slope, measured at Vd=2 V.

with channel length reduction in p-channel than in n-channel MOSFETs is clearly shown[3]. It means that the difference between n- and p-channel MOSFETs' performance becomes smaller in the very short channel region, which could produce better performance balance of CMOS operation in these small devices. Also, we note the deviation from the straight line in 0.1μm regime of n-channel MOSFETs in Fig.4, which may suggest the occurrence of velocity overshoot, though the maximum Gm doesn't reach the υ_{sat}Cox. Next, we will discuss the switching speed measured in the unloaded ring oscillators with 101 stages. Figure 5 shows the gate length dependence of the propagation delay time in the ring oscillator. We have achieved the τ_{pd} of 43 psec/stage in the 0.1μm gate length CMOS ring oscillator. However, we have expected that 0.1μm CMOS should be faster than this value. We have found that this is partly due to the fact that the silicided gate polysilicon resistance has increased with the line width reduction, and partly due to the junction capacitance increase brought about by the additional implantation underneath the original diffused area for the pocket structure. It has been also verified by the circuit simulator, SPICE, that our device should have sub

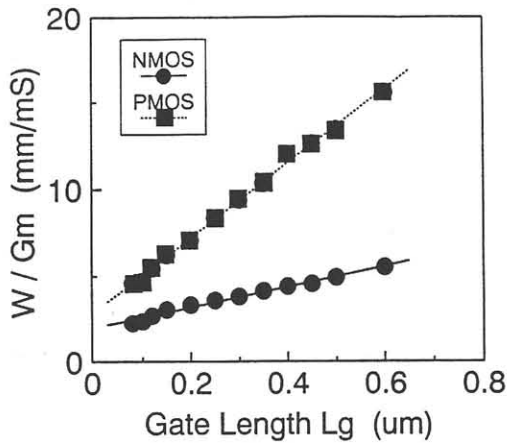

Fig.4 The gate length dependences of the inverse of transconductance for n-ch and p-ch MOSFETs, measured at Vd=2 V.

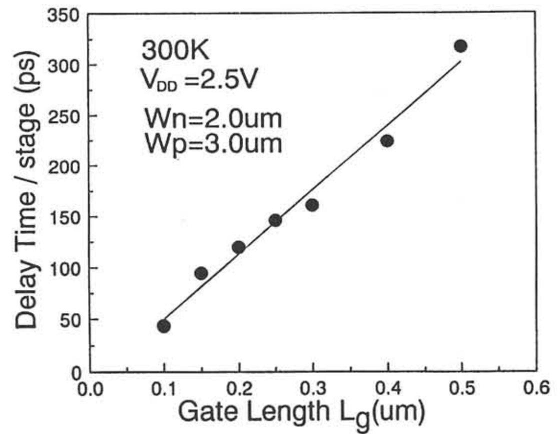

Fig.5 The gate length dependence of propagation delay time in the unloaded ring oscillators, measured at Vdd=2.5 V.

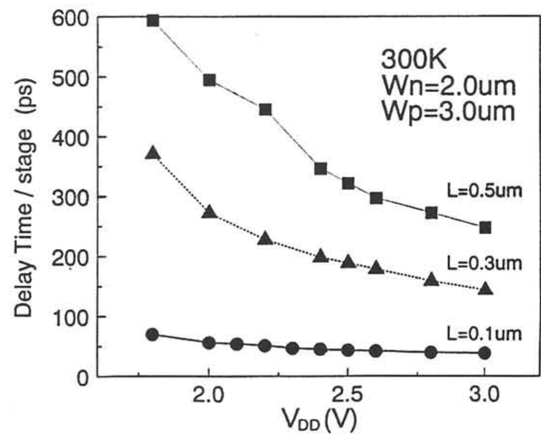

Fig.6 The power supply volatge dependences of propagation delay time for three kinds of gate lengths CMOS ring oscillators.

20 psec/stage by reasonably optimizing the parasitic effects. These results clearly demonstrate the merit of further miniaturization of CMOS devices in terms of both the driving and the speed performance. Furthermore, Fig.6 shows the weak power supply voltage dependence of τ_{pd} in 0.1μm region, compared to the longer channel devices. It can be mainly due to the fact that electrons move along the channel at nearly the saturated velocity. Finally, we would comment that we have found very fast switching speed in the 0.1μm CMOS with relatively low threshold voltages. It is 27 psec/stage at 2.5V, which is the fastest ever reported. Therefore, from the speed as well as the driving performance point of view, we surely believe that 0.1μm CMOS operating at room temperature is quite promising, potentially with even better performance.

4. Conclusion

We have studied the feasibility of 0.1μm CMOS devices operating at room temperature, which have been fabricated without any unconventional process technology. We have not optimized the device design yet, but the merits of miniaturization potentially possessed in CMOS devices down to 0.1μm have been experimentally demonstrated, particularly the very high transconductance and the very fast switching. These results provide a direct evidence in favor of further miniaturization of CMOS devices down to 0.1μm for the room temperature operation.

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