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3 V Operation of 70 nm Gate Length MOSFET with New Double Punchthrough Stopper Structure

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70nm gate length MOSFET with a new double punchthrough stopper structure has been fabricated based on a coupled drain and substrate engineering. This new device shows the reverse short channel effect in addition to the normal short channel effect which is caused by the source-drain punchthrough stopper regions. These short channel effect and the reverse short channel effect were suppressed by optimizing the punchthrough stopping implant and the channel implant conditions. As a result, the small size device with 70nm gate length is successfully operated at 3V supply voltage showing a small cut-off current of 1nA.

1. Introduction

It is a great concern for device researchers what the real limitation in the MOSFET feature size is. It has been said that MOSFET encounters the physical limit at around 20nm channel length which corresponds to 50nm to 70nm gate length in the conventional MOSFET. Aiming to approach such limitation and eventually to overcome it, a few works about small size MOSFET with the gate length $L_G=0.1\mu m$ have been already reported[1)-7)]. However, these small size devices suffer from serious short channel effects and consequently show poor turn-off characteristics when the drain voltage is increased to more than 1.5V or 2V. A considerably large current of several ten μA flows in some $0.1\mu m$ devices reported so far at $V_D=1.5V$ and $V_G=0V$. Thus, it is most important to reduce the short channel effects and to improve the cut-off characteristics for achieving the small size devices with the gate length less than $0.1\mu m$. We demonstrate in this paper that a new MOSFET with $L_G=70nm$ is successfully operated at 3V and shows a very small cut-off current of 1nA.

2. Fabrication Process

Short channel MOSFETs with $L_G=70nm$-500nm were fabricated according to a conventional NMOS process in conjunction with a direct write EB lithography and a new two step ECR plasma etching. The gate oxide thickness was 5nm. The BF_2 punchthrough stop implant with the dose of $1\times10^{13}cm^{-2}$ was carried out through the 10nm sacrificial oxide. The gate electrode was delineated by the direct write EB lithography. The poly-Si was etched with two step ECR plasma etching technique where the anisotropic etching was initially performed to minimize the side etching and then the highly selective etching was done to minimize the reduction of the gate oxide. After poly-Si etching, the 6nm reoxide and the 20nm silicon nitride were formed in the source and drain regions. The $0.1\mu m$ thick poly-Si side wall spacer was formed also by using the two step ECR plasma etching technique. The n^-, n^+ and n^{++} regions were formed by As ion implantation. The n^{++} regions were useful to reduce the diffusion layer resistance. The maximum process temperature was strictly limited less than 850°C. The junction depths of n^-, n^+ and n^{++} regions were around 40nm, 80nm and 160nm, respectively.

3. Device Characteristics

We found that a part of borons in the punchthrough stopper region diffused into the surface of source and drain regions during reoxidation process step. Such oxidation enhanced diffusion is caused by Si self-interstitials generated during the reoxidation. We propose to fabricate a new double punchthrough stopper transistor (DPT) based on a coupled drain and substrate engineering by utilizing this oxidation enhanced diffusion. The cross-sectional view of DPT MOSFET is illustrated in Fig.1 (a) where the punchthrough stoppers around the source and drain edges (SD punchthrough stoppers) are formed by the upward diffusion of borons in the blanket implanted punchthrough stopper (substrate punchthrough stopper) region. Figure 1 (b) is the SEM cross-section of DPT MOSFET with $L_G=70nm$. The I_D- V_D characteristics of this device are shown in Fig.2. It is clear that 70nm DPT MOSFET successfully operates at 3V supply volt-

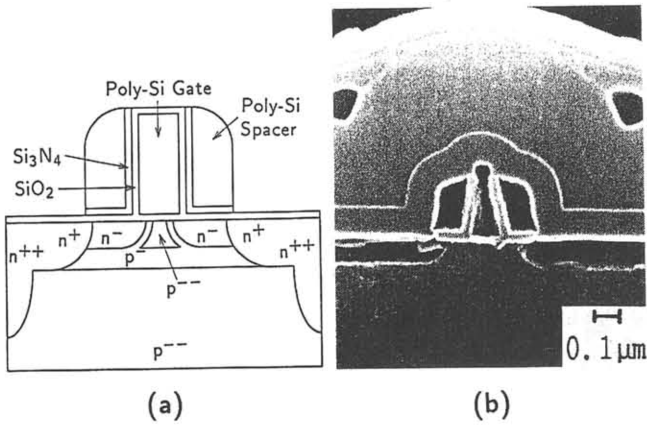


Fig.1 Cross-section of DPT MOSFET.

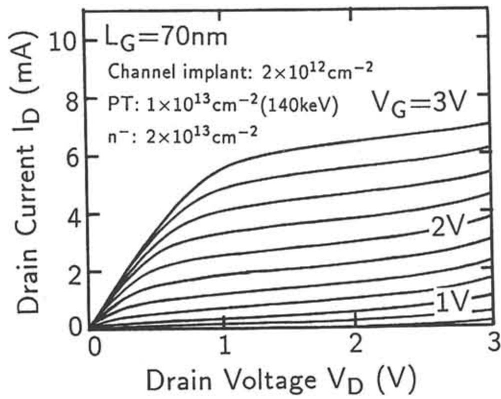


Fig.2 I_D-V_D characteristics.

age. Figure 3 depicts the subthreshold characteristics with V_D=1V which represent excellent turn-off behaviors. The cut-off current at V_G=0V was around 1nA at V_D=3V. Figure 4 shows the L_G dependence of the saturation region threshold voltage V_{th}. The reverse short channel effect where V_{th} is increased with decreasing L_G is observed in the figure. This reverse short channel effect is caused by the SD punchthrough stopper regions. The boron impurity concentration in the channel region is increased by the SD punchthrough stopper regions as L_G is decreased. The reverse short channel effect is mitigated when the blanket implant energy for the substrate punchthrough stopper is increased from 100keV to 140keV, because the substrate punchthrough stopper region becomes deeper. The excellent V_{th}-L_G relation was obtained in DPT MOSFET with channel implant dose of $2\times10^{12}cm^{-2}$ and 140keV implanted punchthrough stopper. The V_{th} is decreased with decreasing L_G in the shorter gate length region due to the normal short channel effect. This short channel effect is more significant in the device with higher channel implant dose. The L_G dependence of the subthreshold swing is plotted in Fig.5. The device with $2\times10^{12}cm^{-2}$ channel implant and 140keV punchthrough stopper again represents the excellent L_G dependence. Figure 6 shows the L_G dependence of the linear region transconductance g_m. As is obvious in the figure, the g_m is increased with reducing the gate length. However, the improvement of g_m by reducing the gate length is less than that

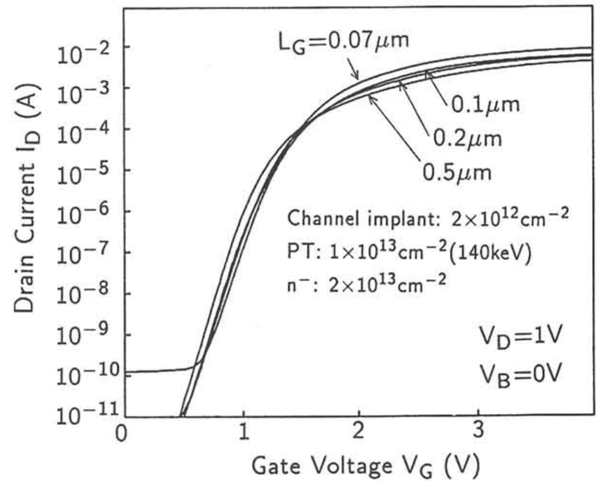
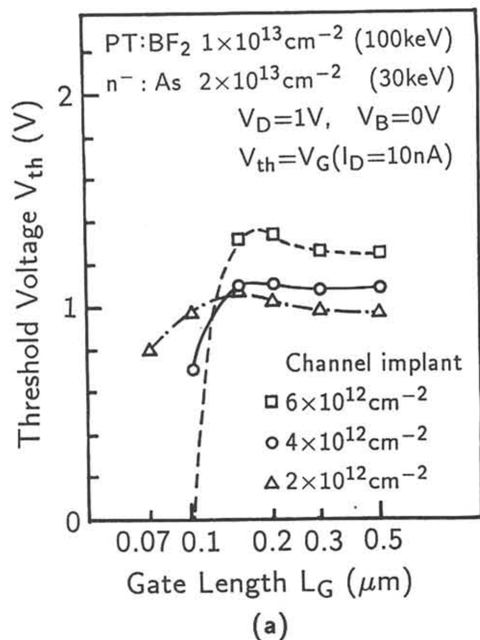


Fig.3 Subthreshold characteristics.



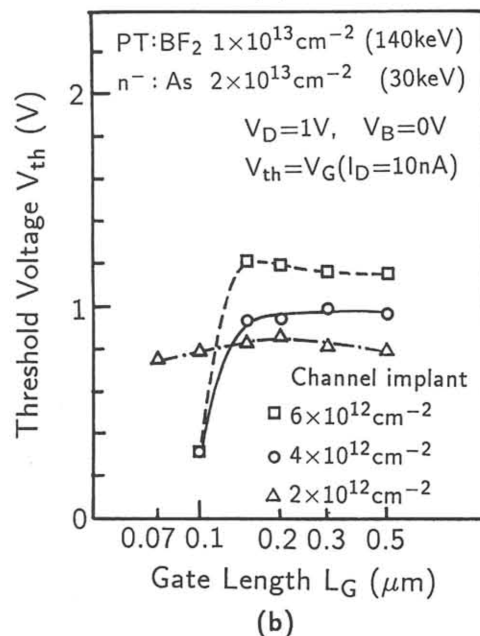


Fig.4 Gate length dependence of threshold voltage.

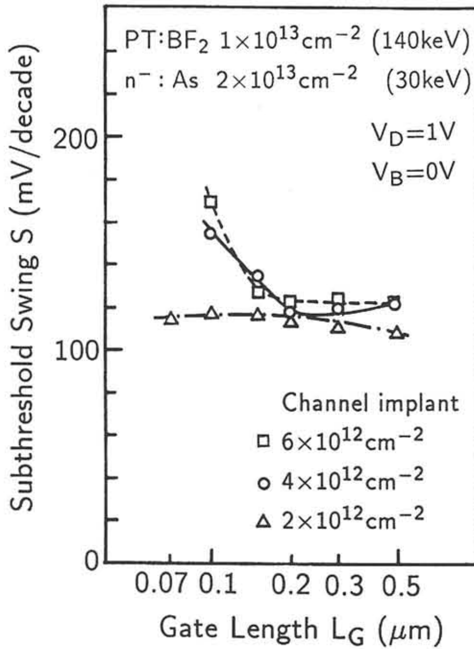


Fig.5 Gate length dependence of subthreshold swing.

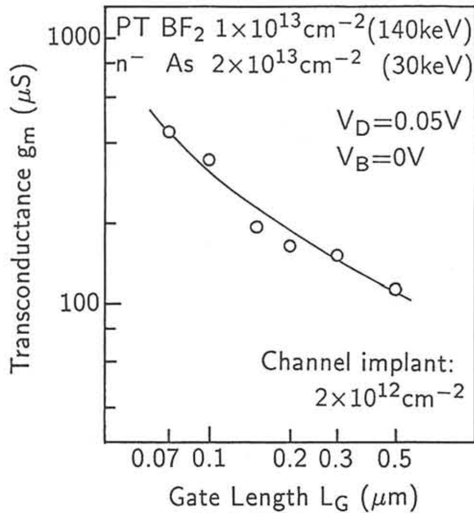


Fig.6 Gate length dependence of transconductance.

prospected from the simulation data. Such relatively limited improvement of g_m in the smaller size devices is caused by the parasitic series resistance and the partially depleted poly-Si gate electrode in addition to the punchthrough stopper region. Particularly, the partially depleted poly-Si gate electrode has a significant influence on g_m, because the impurity doping to the poly-Si gate electrode is carried out only by As ion implantation and the maximum process temperature is limited less than 850°C in our devices. The influence of the depleted poly-Si gate electrode can be evaluated by measuring the C-V curve of MOS diode with n^+ peripheral layer as shown in Fig.7. It is clear in the Fig.7 that the capacitance in the inversion condition is reduced by the depleted poly-Si gate electrode when the annealing is not sufficient. The device fabrication conditions should be further optimized to suppress such depletion of poly-Si gate electrode and to increase the transconductance more significantly.

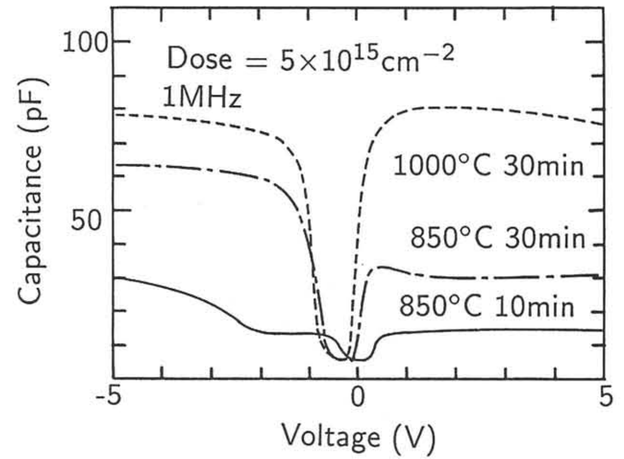


Fig.7 C-V characteristics.

4. Conclusion

The 70nm gate length MOSFET with a new double punchthrough stopper structure is successfully operated at 3V supply voltage. Both the short channel effect and the reverse short channel effect were significantly suppressed by optimizing the punchthrough stopping implant and the channel implant conditions.

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