Extended Abstracts of the 1992 International Conference on Solid State Devices and Materials, Tsukuba, 1992, pp. 493-495

Invited

SOI: New Opportunities for Sub-0.25 μm VLSI

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Scaling of the room temperature CMOS is rapidly approaching its limits. In order to further improve bulk CMOS performance one has either to use SOI or to operate the CMOS at 77K. SOI devices in the 0.25 μm regime and below show significant performance improvement compared with bulk CMOS. This gives SOI the potential of being used as for highest performance room temperature CMOS, provided a number of outstanding problems are solved. SOI has a a clear advantage over bulk for low temperature (77K) operation at a reduced voltage as well. In bipolars, SOI allows realization of devices with no parasitic junction capacitance, sub-0.25 μm emitter widths, easy isolation, and CMOS-like density.

I. INTRODUCTION

Simple bulk silicon has been used as the basic substrate for fabrication since the introduction of integration. Despite many attempts, no other substrate has been able to replace the bulk Si as the VLSI substrate of choice. SOI has been one of the main contenders as an alternative substrate. In a number of key areas SOI offers advantages over bulk Si. Many of these advantages were masked with the rapid progress in scaling of room temperature CMOS. With the slowdown in 300K CMOS scaling, SOI has a real chance of replacing bulk Si.

Room temperature CMOS is being rapidly scaled down into the 0.25 μm range and below. In these channel length regions, very high circuit performances approaching that of bipolar circuits have been obtained. Indeed there is some speculation that it will replace bipolars in the high end systems [1]. For use in such systems, it is imperative that the highest performance CMOS be devised. Figure 1 presents the trend observed in scaling of CMOS. As the the channel length is reduced, speed is improved and the the supply voltage is reduced for reliability reasons. This trend cannot continue indefinitely: One is not able to scale the threshold of the device and ultimately lack of overdrive will result in reduced performance. Presently state of the art CMOS is a 0.25 μm CMOS with a supply of 2.5 V [2]. There will probably be one more 300K CMOS generation with a channel length of about 0.15 μm and a supply voltage somewhere below 2 V. This will likely be the end of bulk CMOS scaling at 300K. In order to further improve the CMOS performance, there are two paths: Use SOI, or scale the threshold by going to 77K. In this paper, it is argued that SOI has some key advantages for use in high performance 300K CMOS for channel lengths of 0.25 μm and below, but a number of key issues must be resolved. Ultimately, to improve on the 300K CMOS, one has to go to low temperature. At 77K, SOI offers enormous advantage over bulk CMOS. In bipolars, SOI allows the realization of devices with very small junction parasitic capacitances, sub-0.25 μm emitter widths, easy isolation, and CMOS-like device area. These feature are especially attractive in a dense high performance BiCMOS technology.

II. SOI FOR 300K CMOS

Background: SOI has been around for many years and except for a few speciality applications, it has failed to take over the main stream CMOS market. Initially this was due to rapid improvements in bulk CMOS (best bulk CMOS was as good as SOI) and bad SOI material quality. Material quality has improved significantly over that last decade. As material quality has improved, effects caused by the floating MOS body have manifested themselves in

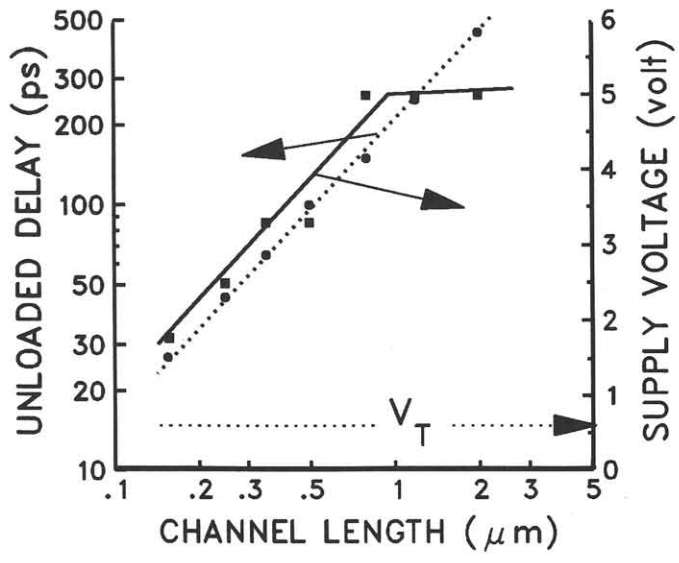

Figure 1: Trends in 300K bulk CMOS.

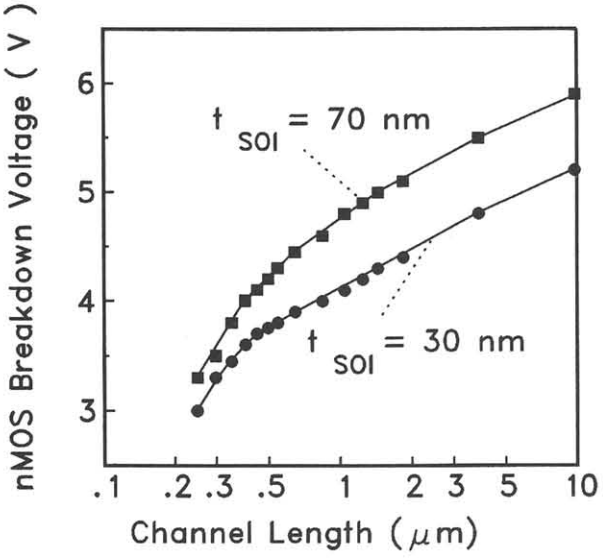

Figure 2: NMOS breakdown at different SOI thicknesses.

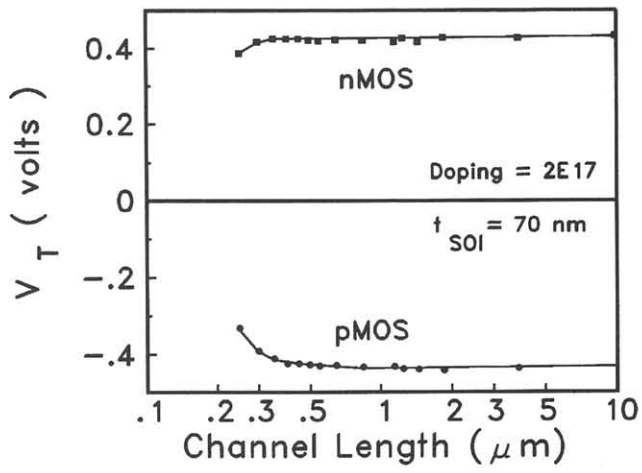

Figure 3: Threshold roll-off for a 300K CMOS on SOI at $V_{DS} = 0.1\ V$.

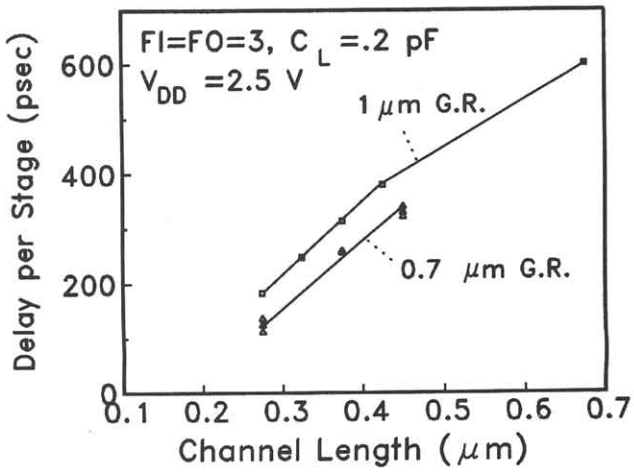

Figure 4: Loaded 3-way NAND performance *vs.* channel length for two layout ground rules.

more severe forms. These effects have led to complications in design of devices and circuits.

SOI Material: Many methods to obtain SOI have been devised [3]. Among the more promising techniques are wafer bonding, SIMOX, and epitaxial lateral over growth and chemical mechanical polishing (ELO + CMP). In the last few years the defect density for some of these methods has gone down from $10^6\ cm^{-2}$ to less than $10^3\ cm^{-2}$. Low defect density SOI films prepared by many of these techniques are commercially available. Some fairly complicated circuits on SOI with low standby currents have been fabricated. This is indicative of the good quality and low leakage material. Emphasise has shifted to acquiring good thickness control for operation of fully depleted MOS devices. It will later be argued that this is unnecessary. In summary material quality no longer seems to be the barrier to the use of SOI.

Design Point for 300K CMOS: There are two main floating body effects: The kink effect and reduced device breakdown. In order to eliminate the kink effect, use of fully depleted ultra-thin SOI has been widely investigated. It has furthermore been argued that ultra-thin SOI improves the short channel effects and the hot electron problem. There are however a number of problems with ultra-thin SOI: It makes the device threshold, V_T, dependent on SOI thickness. As doping is raised to reduce the SCE in deep submicron range, use of fully depleted SOI leads to very stringent control on SOI thickness [4]. It has been suggested that ultra-thin SOI improves the SCE: The observed improvement is due to reduction of junction depth. In fact for the same junction depth, device SCE is *worse* on SOI compared to bulk Si. Hot electron effect also does not improve on SOI compared to bulk. For the same overdrive ($V_{GS} - V_T$) SOI devices have higher peak lateral field and worse hot electron effects. One of the issues associated with using SOI has been reduced nMOS breakdown. This problem worsens with using ultra-thin SOI. Figure 2 is a plot of breakdown *vs.* channel length for 2 different SOI thicknesses: Reducing the thickness leads to lower breakdown voltage. Probably the biggest barrier to ultra-thin fully depleted SOI is that it does not allow use of tailored channel implant to reduce SCE in the sub-0.2 μm range [5, 6]. Judging from the doping and breakdown requirements for sub-0.25 μm CMOS, CMOS on SOI devices will be un-depleted, but the SOI will be thin enough to eliminate junction capacitance and isolate the channel. The kink effect will not be an issue for digital circuits. For analog circuits (i.e. sense amps) it leads to offset voltages higher than bulk circuits. In case this turns out to be a problem, one may selectively put some key devices on bulk, i.e. use a method to obtain SOI which allows one to get both SOI and bulk Si on the same wafer (such as ELO + CMP [4]).

A High Performance 300K CMOS on SOI: In the literature a vast class of circuits on SOI have been fabricated, and speed enhancement factors of 1.1-3× compared to bulk have been obtained. Using SOI, a high performance 0.25 μm 300K CMOS has been fabricated. Figure 3 shows the threshold roll-off at $V_{DS} = 0.1\ V$. The background doping is $2 \times 10^{17}\ cm^{-3}$, SOI thickness is 70 nm, and the gate oxide thickness is 7 nm. Figure 4 is the delay per stage *vs.* the channel length ($\frac{L_n + L_p}{2}$) for a 3-way NAND (FI=FO=3, C_L=0.2 pF), for 2 different ground rules. Loaded 3-way NAND delays approaching 120 *psec* have been obtained. A significant part of the speed improvement is due to elimination of junction capacitance and the body effect. Both

of these factors will become more important as one scales further into the sub-0.25 μm regime.

Outstanding Issues for 300K CMOS on SOI: The biggest barrier to widespread use of SOI has been the steady improvement in bulk CMOS, but bulk CMOS is rapidly approaching its limits. This presents SOI with an opportunity for replacing bulk Si. There are a number of problems that must be addressed first: Floating body effects and self-heating effects, especially in the transient mode and their effect on analog circuits needs further study. Low device breakdown, burn-in and testing of CMOS on SOI is an important issue. Hot electron effects and the question of supply voltage are the remaining issues. In general, there is a need for careful evaluation and understanding of a variety of CMOS circuits on SOI, especially in the presence of floating body effects, and low breakdown nMOS.

III. SOI FOR 77K OPERATION

Background: Ultimately to improve on the 300K CMOS and move into the deep sub-micron CMOS regime, one has to scale the threshold voltage. Low temperature (77K) operation of CMOS devices allows the scaling of the device threshold and therefore reliable operation of sub-0.25 μm devices. At low temperature, the optimum operating point for CMOS devices includes both a reduced power supply and reduced threshold voltage. In bulk CMOS, it is difficult to achieve low V_T with the high doping necessary to obtain acceptable SCE. Ultra-thin silicon on insulator ($t_{SOI} \ll t_{depletion}$) offers the possibility of obtaining low V_T at 77K while keeping the channel doping high. This is due to reduction of the depletion charge.

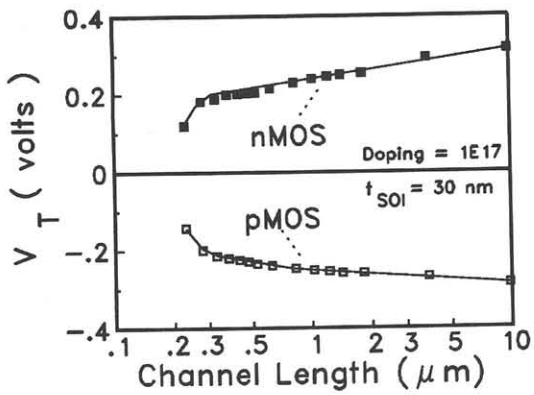

Figure 5: Threshold roll-off for a 77K CMOS on SOI at $V_{DS} = 0.1\ V$.

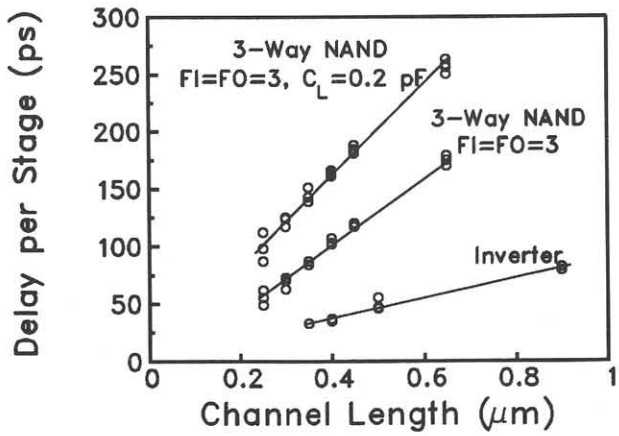

Figure 6: 77K CMOS on SOI delay.

77K CMOS on SOI: Deep submicron CMOS was fabricated on ultra-thin SIMOX films [7]. Figure 5 shows the threshold roll-off. The threshold voltages are optimum for a 0.3 μm 77K CMOS on SOI. The SOI electrical film thickness is 30 nm and the film doping is $1 \times 10^{17}\ cm^{-3}$. Figure 6 is the measured delay for various loadings *vs.* the channel length. For 0.25 μm channel length, loaded 3-way NAND delays below 100 psec at V_{DD} of 2 volts has been obtained [7].

Discussion: Using SOI, very fast loaded operation at 77K has been demonstrated. Performances are close to the expected 0.1 μm bulk 77K CMOS, but obtained at longer channel length. This shows that ultimately for 77K CMOS, SOI offers significant performance advantage over bulk.

IV. BIPOLAR and BICMOS ON SOI

The integration level and practical performance of bipolar ECL circuits are limited by the chip power dissipation. SOI offers possibility of some novel bipolar structures with deep submicron emitter widths, minimum capacitances, and CMOS footprint. One such structure is shown in Fig. 7. It has f_T of over 20 *GHz*, low base, collector and emitter resistances and capacitances [8]. Isolation on SOI is a much easier task and fabrication of BiCMOS and complementary BiCMOS structures becomes much simpler.

V. SUMMARY

It has been argued that SOI offers some key advantages in a wide variety of devices in sub-0.25 μm VLSI where scaling of bulk 300K CMOS is approaching its limits. SOI presents the opportunity of improving the 300K CMOS performance. Ultimately one is forced to go to low temperature to improve on 300K CMOS. At 77K, in a reduced voltage environment, SOI has clear advantages over bulk silicon. Finally SOI can be used to make some novel and potentially high performance bipolar devices.

VI. REFERENCES

1. A. Masaki, *VLSI Symp. Tech. Dig.*, (1991) 1.
2. B. Davari *et al*, *IEDM Tech. Dig.*, (1988) 56.
3. Silicon-on-Insulator, *IEDM Short Course*, (1990).
4. G. Shahidi *et al*, *IEDM Tech. Dig.*, (1990) 587.
5. G. Shahidi *et al*, *IEEE EDL-9*, (1988) 94.
6. G. Shahidi *et al*, *DRC Tech. Dig.*, (1989) 54.
7. G. Shahidi *et al*, *VLSI Symp. Tech. Dig.*, (1992) 106.
8. G. Shahidi *et al*, *IEDM Tech. Dig.*, (1991) 663.

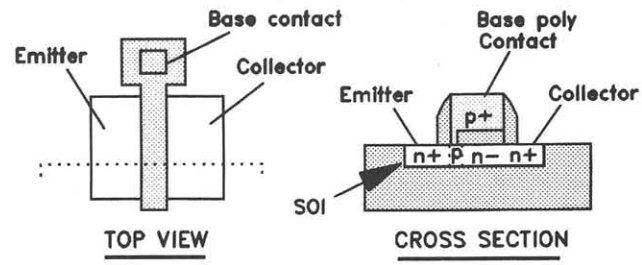

Figure 7: Lateral bipolar structure on SOI.