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Hot-Carrier Immunity of a 0.1-μm-Gate Ultrathin-Film MOSFET/SIMOX

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It is shown experimentally that the substrate current decreases with the decreasing silicon layer thickness in contrast to past simulation results reported[4]. It is also discussed that the substrate current may be suppressed through the velocity overshoot effect in extremely short-channel devices.

It is shown that, at least, the structural optimization for suppressing the short-channel effect in ultrathin-film SOI devices does not always degrade the lifetime in contrast to bulk devices.

1. INTRODUCTION

Fully-depleted ultrathin-film devices are attracting attention because of short-channel effect suppression and high-speed performance[1]. This has been shown by the superior results obtained by SIMOX technology recently[2]. In these days, hot carrier immunity of SOI devices is widely under discussion[3], although few basic investigations are reported on the relation between structural parameters and degradation.

This paper describes the nature of the maximum substrate current ($I_{SUB(max)}$) of ultrathin-film MOSFETs/SIMOX for various structural parameter values. Furthermore, the relationship between the basic characteristics and the degradation is discussed.

2. DEVICE FABRICATION AND STRESSING

CMOS/SIMOX devices were fabricated on SIMOX substrates with a 480-nm-thick or 80-nm-thick buried oxide layer. Gate oxide thickness (t_{ox}) was 7-nm. N-type polysilicon was used for gate electrodes. Source and drain regions were formed by ion implantation after gate spacer formation. Therefore, an LDD-like structure was built in beneath the gate spacer. The silicon layer thickness (t_s) was varied between 30 nm and 100 nm.

Some devices had body contacts for measuring the substrate current. Typical substrate current (I_{SUB}) and drain current (I_D) dependences on gate voltage (V_G) are shown in Fig. 1. $I_{SUB(max)}$ locates near the threshold voltage; $V_G \sim V_{TH}+0.2$, which is almost independent of drain voltage (V_D). This is a significant feature in contrast to bulk devices. Stress was applied to devices at the bias point where I_{SUB} takes the maximum value. The lifetime was specified by g_m degradation because it was larger than V_{TH} degradation.

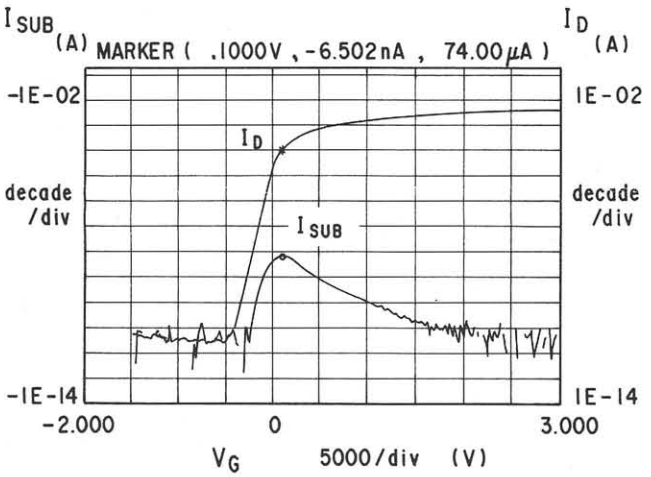

Fig. 1. I_{SUB} and I_D dependences on gate voltage for 0.4-μm-gate nMOSFET at V_D of 2.5V.

3. RESULTS AND DISCUSSION

3.1 Features of substrate current

The authors previously proposed a design concept for a 0.1-μm-gate CMOS/SOI[2]. This approach consists in thinning both the silicon layer and the buried oxide layer which is indispensable to suppress the short-

channel effect. To achieve this, the buried oxide layer thickness (t_{BOX}) should be smaller than gate length (L_G).[4] However, numerical simulations by Choi et al.[4] have warned against increasing the substrate current in the case of decreasing t_s.

We measured the substrate current characteristics using the fabricated MOSFETs/SIMOX. $I_{SUB(max)}/I_D$ values are shown in Fig. 2. $I_{SUB(max)}/I_D$ increases with decreasing t_{BOX}. However, it decreases with decreasing t_s. The validity of these data is confirmed by the evaluation of device characteristics degradation. This figure suggests that we can suppress the increase in $I_{SUB(max)}/I_D$ by optimizing structural parameters. Our experimental results seem to indicate that the multiple factor in the avalanche phenomenon has been overestimated in the previous simulations[4]; it can be suggested that the surface avalanche factor becomes more dominant than the bulk avalanche factor as t_s decreases[5].

Next, $I_{SUB(max)}/I_D$ dependence on L_G is shown in Fig. 3. To discuss the nature of $I_{SUB(max)}/I_D$, we also evaluated the effective carrier velocity as shown in Fig. 4. $I_{SUB(max)}/I_D$ increases with decreasing L_G, up to a peak value of around 0.2 μm-long gate, because of the increase of internal electric field at a time. However, $I_{SUB(max)}/I_D$ decreases with decreasing L_G thereafter. In case of bulk devices, recently, it is reported that the substrate current in the extremely short channel device decreases by the ionization rate suppression due to the velocity overshoot effect of channel carriers[6]. It can be easily speculated that the identical phenomenon takes place in such short-channel SOI devices.

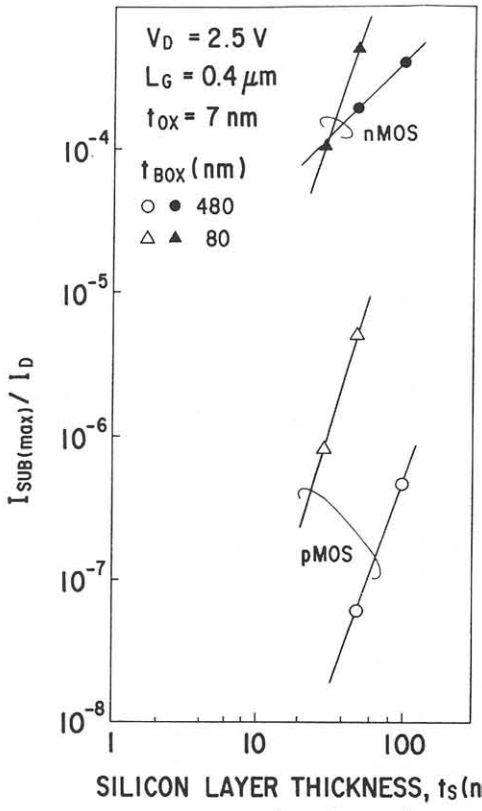

Fig. 2. $I_{SUB(max)}/I_D$ dependence on silicon layer thickness for nMOSFETs and pMOSFETs.

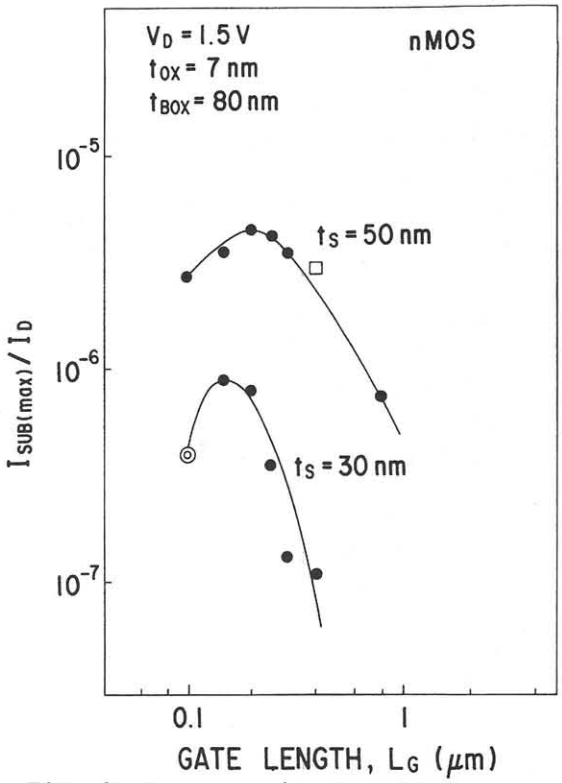

Fig. 3. $I_{SUB(max)}/I_D$ dependence on gate length for nMOSFETs with two different silicon layer thicknesses. Symbols "□" and "◎" correspond to representative devices focused on for the following discussion.

3.2 General aspects of hot-carrier degradation

The lifetime dependences on $1/V_D$ for 0.4-μm-gate nMOSFETs/SIMOX are shown in Fig. 5. Some devices have zero-biased body contacts. Lifetime was specified by g_m degradation. Degraded portion was almost limited in the LDD-like region near the drain. Degradation was hardly found at the silicon-buried oxide interface. There is not a significant difference in lifetime between the device with the body contact and those without it. Therefore, it can be considered that holes don't play an important role in the degradation process. The device has a 10-year lifetime at V_D of 1.7 V according to the extrapolation of the measured lifetimes.

3.3 Hot-carrier immunity of 0.1-μm-gate nMOSFET/SIMOX

The lifetime dependence on $1/V_D$ is shown in Fig. 6 for a 0.1-μm-gate nMOSFET/SIMOX with a 30-nm-thick silicon layer and an 80-nm-thick buried oxide. The lifetime was specified by the gm degradation. The device has a 10-year lifetime at V_D of 1.6 V according to the extrapolation. It can be seen that lifetimes of these devices in Figs. 5 and 6 are almost identical. To discuss this point, the $I_{SUB(max)}/I_D$ dependence on L_G shown in Fig. 3 can be used. The symbols "□" and "◎" correspond to a 0.4-μm-gate nMOSFET in Fig.

5 and a 0.1-μm-gate nMOSFET in Fig. 6, respectively. It is usually believed that the degradation of the device characteristics is strongly correlated to $I_{SUB(max)}/I_D$. This conventional idea is no longer valid. Such result leads us to think of a new degradation mode for a 0.1-μm-gate nMOSFET/SIMOX.

Nevertheless, from the fact that the lifetimes of 0.1-μm- and 0.4-μm-gate nMOSFETs/SIMOX are identical, it can be said that, at least, the structural optimization for suppressing the short-channel effect does not always degrade the lifetime of SOI devices. This is a strong encouragement for the development of future giga-scale ULSIs.

4. CONCLUSION

It has been found experimentally that $I_{SUB(max)}/I_D$ decreases with decreasing t_s in contrast to past simulation results. It has been proposed qualitatively that the substrate current may be suppressed through the velocity overshoot effect in extremely short-channel devices.

It has been concluded that, at least, the structural optimization for suppressing the short-channel effect does not always degrade the lifetime of SOI devices. These encouraging results are promising for the future development of giga-scale ULSIs.

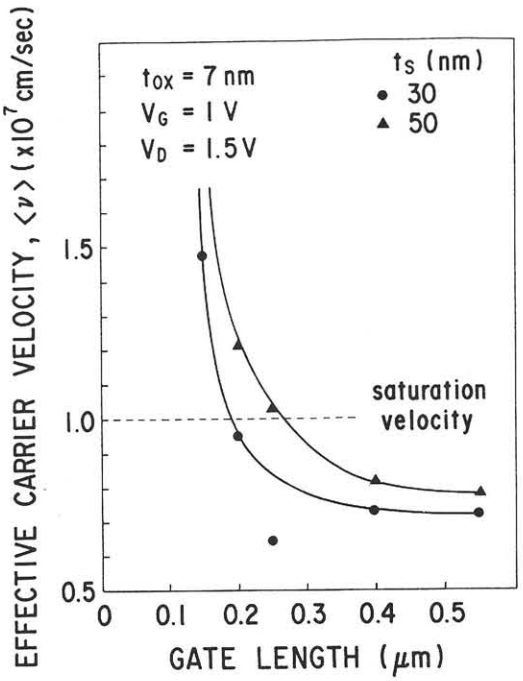

Fig. 4. Effective carrier velocity evaluated for nMOSFETs with two different silicon layer thicknesses. $\langle v\rangle = g_{mi}/WC_{ox}$.

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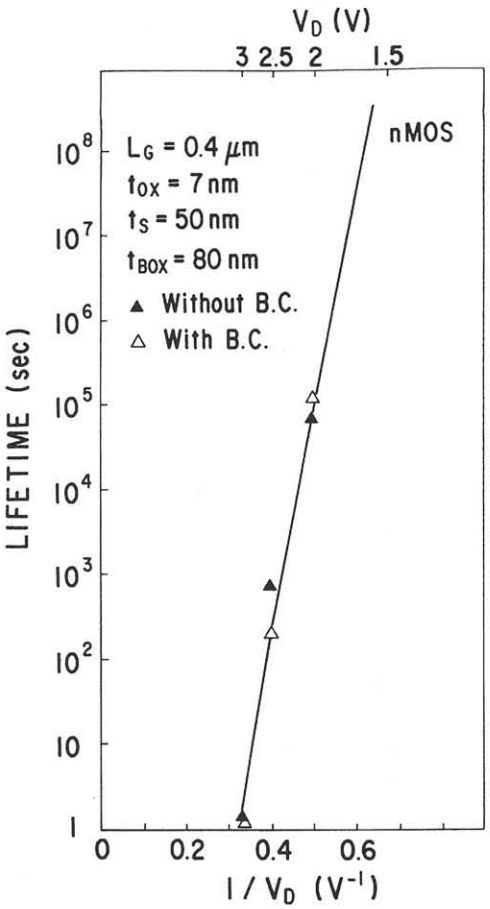

Fig. 5. Lifetime dependence of 0.4-μm-gate nMOSFET on inverse drain voltage.
B.C.: body contacts

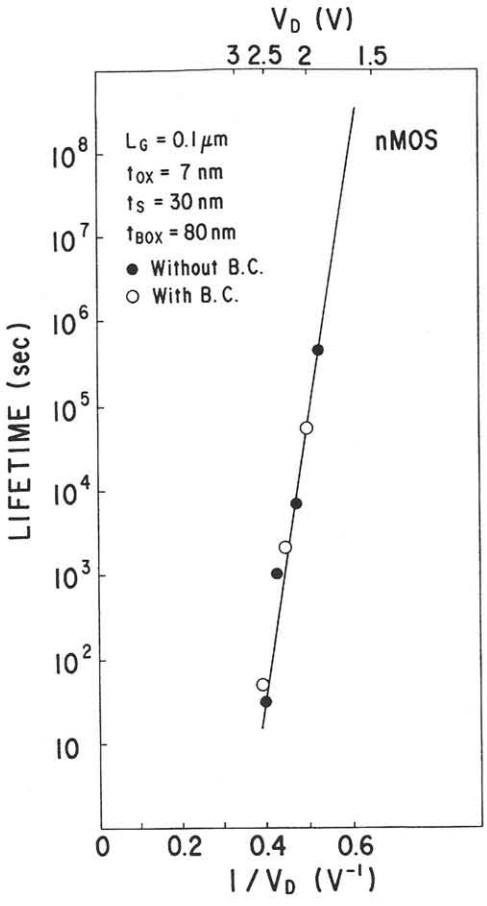

Fig. 6. Lifetime dependence of 0.1-μm-gate nMOSFET on inverse drain voltage.
B.C.: body contacts