Extended Abstracts of the 1992 International Conference on Solid State Devices and Materials, Tsukuba, 1992, pp. 502-504

Sub-20 psec Switching CMOS at Liquid N_2 Temperature

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Abstract: We have investigated the performance and characteristics of 0.2μm CMOS devices designed for operating at cryogenic temperature. It is stressed that the low surface impurity concentration should be essential for the cryogenic operation from a standpoint of making the best use of the improvement of the short channel effects at low temperature. The fastest speed performance of 0.2μm Cryo CMOS operating with a low power-supply voltage has been experimentally demonstrated; 19.8psec at V_{dd}=2V and 23psec at V_{dd}=1V. We have found that this high-speed performance is owing largely to the reduction of the gate electrode resistance with self-aligned silicide process.

1. INTRODUCTION

Several performance improvements have been pointed out for the low temperature operation of CMOS devices, such as steeper subthreshold swing and higher transconductance. In particular, steeper subthreshold swing makes a low threshold voltage available and provides the possibility of greatly reduced power-supply voltage. In this case, it is very important to suppress the short channel effects with a threshold voltage as low as 0.2V. However, it is not clear whether the reduction of threshold voltage is really possible in the deep-1/4-micron region, and the substantial advantages of the cryogenic operation have not been demonstrated in this region yet.

Furthermore, it has been reported that the short channel effects are improved in the cryogenic operation[1-2]. This indicates that devices can be made smaller and more highly integrated at low temperature than at room temperature. However, an experimental approach toward the improvement of the short channel effects at low temperature has not been fully performed yet.

In this paper, we have experimentally investigated the improvement of the short channel effects at low temperature. Also, we report the excellent performance of 0.2μm Cryo CMOS devices designed for operating at cryogenic temperature.

2. EXPERIMENTAL

Fig.1 shows the V_{th} lowering of n-MOSFETs with the uniform substrate concentration; (a) $5\times10^{15}cm^{-3}$ and (b) $1\times10^{17}cm^{-3}$. The gate oxide thickness was 20nm. It is noted that a pronounced improvement in the V_{th} lowering is observed at 80K on the substrate with the lower impurity concentration, and that there is little difference between the results at 80K and 300K on the substrate with the higher impurity concentration. Consequently, it was found that the low surface impurity concentration is required for the improvement of the short channel effects at low temperature. In addition, this low surface impurity concentration makes it possible to set a low desirable threshold voltage. Therefore, we propose that the low surface impurity concentration should be essential for the cryogenic operation.

A schematic cross section of the device used in this study is shown in Fig.2. The double implanted MOSFETs, which have p^-/n^- regions for the punch-through stopper, were adopted to realize a low surface impurity concentration. Electron-beam lithography and highly selective RIE were utilized to define fine gate electrodes, and surface-channel type n- and p-MOSFETs were fabricated to remove the carrier freeze-out effects. Self-aligned titanium silicide process was employed to reduce the parasitic resistances of gate electrodes as well as source/drain regions.

A twin-well was formed on the n-type (100) substrate with 1-2Ω·cm. The n- and p-well concentration were $3\times10^{16}cm^{-3}$ and $5\times10^{16}cm^{-3}$, respectively. After LOCOS-type isolation, gate electrodes were defined without any channel ion implantation. The gate oxide thickness was 6nm. After the formation of n^+ and p^+ regions, p^- and n^- regions were formed by the rotated 30° tilt angle ion implantation at 130KeV energy. The implantation dose was $2\times10^{12}cm^{-2}$ for BF_2 and $4\times10^{12}cm^{-2}$ for phosphorous. These conditions were chosen so that the peak position of the doping profile was adjusted near the source/drain junctions with the peak concentration of $2\times10^{17}cm^{-3}$ in each region. After rapid thermal annealing at 1000°C for 20sec, self-aligned silicide process using $TiSi_2$ was employed. The final $TiSi_2$ thickness was 50nm.

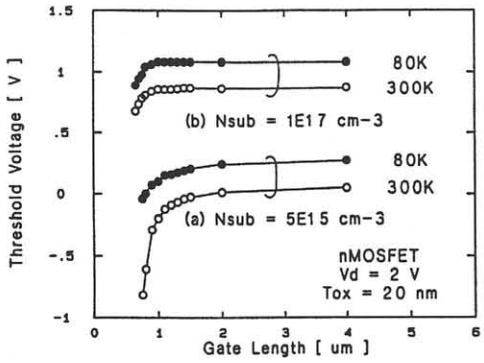

Fig.1 The V_{th} lowering of n-MOSFETs with the uniform substrate concentration; (a) $5\times10^{15}cm^{-3}$ and (b) $1\times10^{17}cm^{-3}$. A pronounced improvement in the short channel effect is observed at 80K on the substrate with the lower impurity concentration.

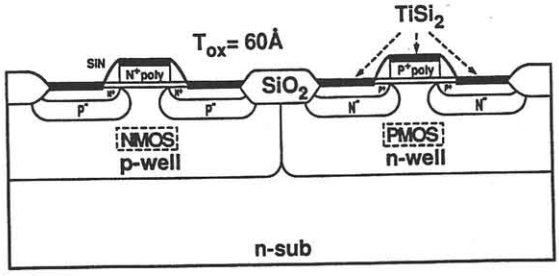

Fig.2 Schematic cross section of the device used in this study. Surface-channel type n- and p-MOSFETs with single drain structure were fabricated.

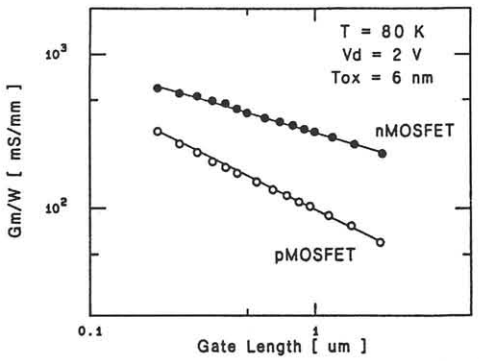

Fig.3 The measured transconductance in the saturation region at 80K. The transconductance increases monotonically with decreasing gate length for n- and p-MOSFETs.

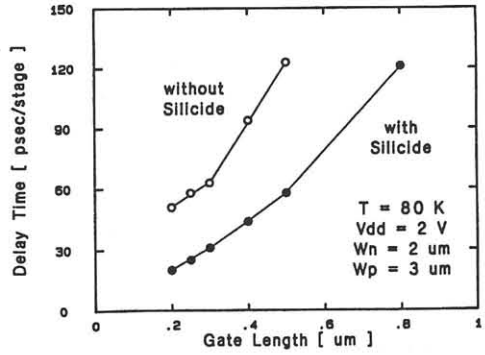

Fig.4 The measured delay time of CMOS ring oscillators at 80K. The significant improvement of delay time is observed with self-aligned silicide process.

3. RESULTS AND DISCUSSION

The short channel effects are improved at 80K and well suppressed down to 0.2μm gate length owing to the careful design of p^-/n^- regions for the punch-through stopper. Moreover, the magnitude of the threshold voltage as low as 0.2V is obtained at 80K, which is necessary to reduce the power-supply voltage.

The peak field-effect mobilities at 80K were as high as 1500 and $300cm^2$/V-sec for n- and p-MOSFETs, improved by a factor of 3.0 and 2.7 compared with those at 300K, respectively. The transconductances in the saturation region were 600 and 310mS/mm for 0.2μm n- and p-MOSFETs, respectively, as shown in Fig.3. It is noted that the transconductance increases monotonically with decreasing gate length for both n- and p-MOSFETs, and that the saturation of the transconductance is not observed until 0.2μm gate length. We believe that the further miniaturization of MOSFETs down to 0.1μm gate length leads to higher performance of Cryo CMOS.

In order to study the speed performance of CMOS devices in the cryogenic operation, CMOS ring oscillators were fabricated and gate delay time was measured. Fig.4 shows the measured propagation delay time of CMOS ring oscillators (F/O=1) at 80K. Each ring oscillator consists of 101 CMOS inverter stages, and the channel widths used in each inverter are 2μm and 3μm for n- and p-MOSFETs, respectively. It is noted that the significant improvement of delay time can be realized with silicide process.

In order to examine the origin of this improvement thoroughly, simulations were carried out, using the circuit simulator SPICE. The device parameters were extracted from the measured I-V characteristics at each gate length, and the parasitic effects were also taken into account. The simulated results are shown in Fig.5. The improvement of delay time cannot be fully explained only by considering the increase of the drain current (10% increase in this study) due to the reduction of the sheet resistance in the source/drain region (CASE 1). In CASE 2, the reduction of the gate electrode resistance, as shown in Fig.6, is also taken into consideration as well as the increase of the drain current. It was clarified that the significant improvement of delay time is mainly due to the reduction of 3 orders of magnitude of the gate resistance with silicide process. We would point out that the difference of temperature dependence between implanted poly-Si and silicided poly-Si causes the improvement in performance to increase with decreasing temperature. This is another advantage for using silicide process in the cryogenic operation.

Fig.7 illustrates an output waveform of 0.2μm CMOS ring oscillator with silicide process at 2V supply voltage. We believe that 19.8psec at V_{dd}=2V is the fastest switching speed among any unloaded CMOS ring oscillators ever reported.

Fig.8 shows the power-supply voltage versus the gate delay time for various gate length MOSFETs. It

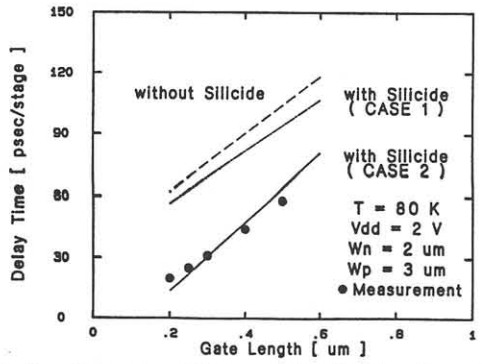

Fig.5 The simulated results of delay time. In CASE 1, only the increase of the drain current due to the reduction of the sheet resistance in the source/drain region is taken into account. In CASE 2, the reduction of the gate resistance is also considered.

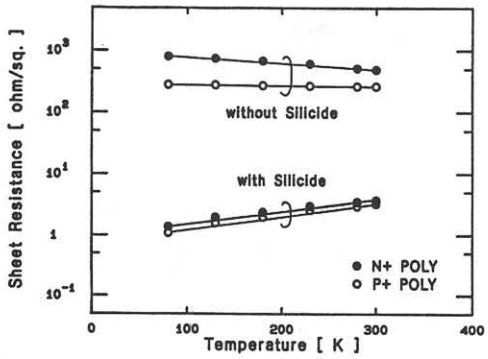

Fig.6 The temperature dependence of gate resistance with/without silicide process. The gate resistance is reduced by 3 orders of magnitude with silicide process.

is noted that the delay time is almost independent of power-supply voltage in the case of 0.2μm CMOS, while it sharply decreases with decreasing power-supply voltage in the case of 0.5μm CMOS. This is because the drain voltage to attain the critical electric field for the velocity saturation is so low for short channel devices, as shown in Fig.9, where the saturation drain voltage V_{dsat} was experimentally determined by the method proposed by Chan et al.[3]. Consequently, the high-speed performance has been achieved for 0.2μm ring oscillator even with an extremely low power-supply voltage; 23psec at V_{dd}=1V and 21psec at V_{dd}=1.5V.

4. CONCLUSION

The fastest speed performance of 0.2μm Cryo CMOS operating with a low power-supply voltage has been experimentally achieved. This clearly demonstrates that the miniaturization of MOSFETs provides not only the high packing density of CMOS LSI, but also the possibility of high speed CMOS with greatly reduced power-supply voltage in the cryogenic operation. We believe that higher speed performance can be realized by the further miniaturization down to 0.1μm. It is concluded that CMOS devices operating at cryogenic temperatures give great promise for future high performance Si-ULSI.

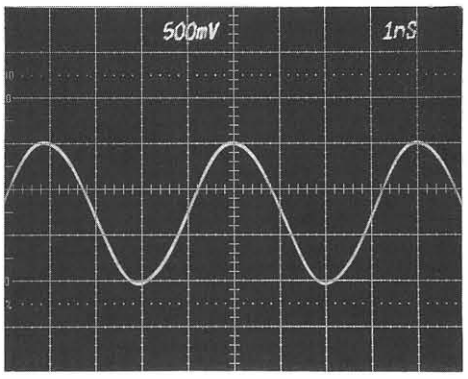

Fig.7 An output waveform of 0.2μm CMOS ring oscillator at 80K. τ_{pd} = 19.8psec at 2V supply voltage.

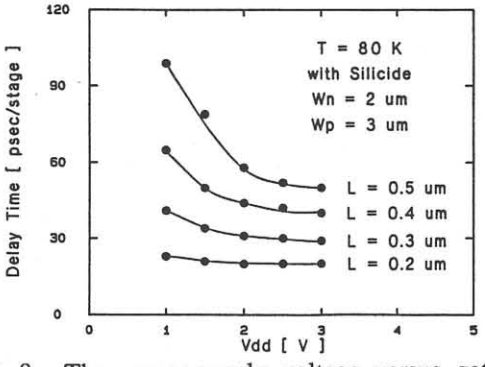

Fig.8 The power-supply voltage versus gate delay time for various gate length MOSFETs at 80K. The high-speed performance has been achieved for 0.2μm ring oscillator even with an extremely low power-supply voltage.

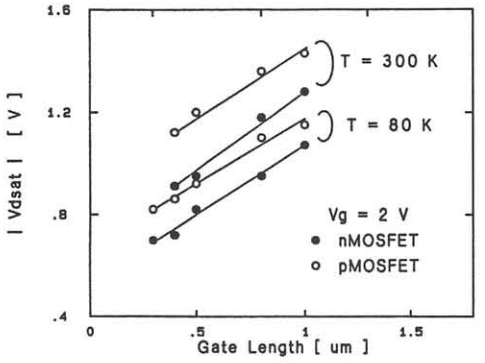

Fig.9 The measured saturation drain voltage versus gate length at 80K and 300K. V_{dsat} decreases with decreasing gate length.

ACKNOWLEDGEMENT

The authers would like to thank M. Yoshimi and I. Mori for their support through this work.

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