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Invited

Proposal of Adaptive-Learning Neuron Circuits with High Density Synapse Array of Ferroelectric Thin Films

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Adaptive-learning neuron circuits are proposed, in which a pulse frequency modulation (PFM) system is used and the interval of output pulses is changed through the learning process. Key devices of the circuits are MISFETs with ferroelectric gate insulator films. They are used for representing the synaptic weights of electical neurons and the polarity of the films is gradually changed by applying input pulses to the gates. In order to produce PFM signals, circuits using a UJT (unijunction transistor) and a PUT (programable UJT) are discussed. For the multiple-input neuron circuits, it is proposed that the adaptive-learning MISFETs be connected in parallel and the FET matrix representating the synapse array between two neuron-layers be realized in high density using an SOI (silicon-on-insulator) structure. Finally, the stability of the feedback-type adaptive-learning neural network is discussed.

1. Introduction

In future neural networks, it will be desirable for the synaptic weight between neurons to be changed through the adaptive-learning process. Here, the term "adaptive learning" is defined as a function in which electrical or optical properties of a device are changed partially or totally after the device has processed a certain number of the usual signals.

I have proposed that digital and analog neuron circuits can be fabricated using ferroelectric thin films deposited on semiconductor substrates[1,2] and that the circuits are particularly suitable for realizing the adaptive-learning function[1]. In this presentation, I review the outline of the adaptive-learning neuron circuits and discuss the stability of the circuit when it is used as a feedback-type neural network.

2. Neuron Circuits

A key component for realizing the adaptive-learning function is a MISFET with a ferroelectric gate insulator film. In this device, the ferroelectric film thickness is so chosen that the polarization of the film is gradually changed by applying signal pulses. In other words, the duration of input pulses is chosen shorter than the switching time for polarization reversal. Thus, the threshold voltage or the source-drain (S-D) resistance of the FET is changed, as the number of input pulses increases.

In the adaptive-learning MISFET (AL-FET), input pulse signals are applied to the gate electrode, while the learned results are given analoglike as variation of the threshold voltage or the S-D resistance. In order to combine two concepts of the pulse input and the analog output, I propose use of a PFM (pulse frequency modulation) system, in which asynchronous short pulses are generated. A basic circuit is shown in Fig.1(a) in which a unijunction transistor (UJT) is used as a switch to discharge the capacitance C and the pulse interval is proportional to CR_1. Therefore, if R_1 is replaced by the S-D resistance of the AL-FET, it is possible to change the output pulse interval of the neuron circuit.

In order to reduce the power consumption in the neuron circuit, it seems to be better to replace the UJT with a PUT (programmable UJT), which is a kind of thyristor with a pnpn structure. The new circuit is shown in Fig.1(b). Since a PUT contains a reverse-biased pn junction, and since it is possible to choose the resistors R_2 and R_3 high, the leakage current in the circuit in Fig.1(b) is expected to be much lower than that in Fig.1(a). In any case, since a positive feedback device such as a UJT or a PUT is included in the circuit, it is necessary that the circuit be fabricated in an SOI (silicon-on-insulator) structure, and that each device be electrically isolated so that the circuit is not latched-up.

Figure 2 shows an example of the optically connected neuron circuits with excitatory and inhibitory synapses.

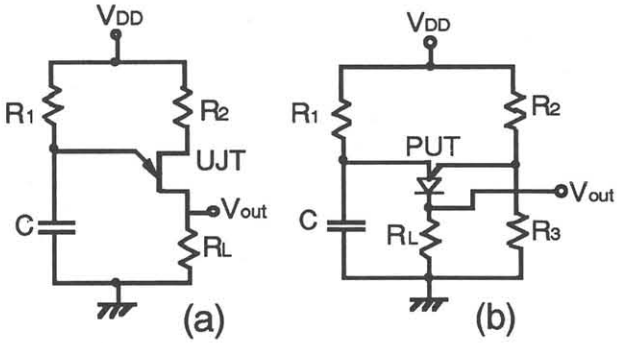

Fig.1. Basic neuron circuits using (a) UJT and (b) PUT.

In this circuit, the resistor R_1 in Fig.1(a) is replaced by AL-FET and R_L is replaced by an LED. Two photoconductors (PCs) connected to the gate of AL-FET are used as switches for applying the positive and negative supply voltages ($\pm V_0$) to the gate, and for changing the S-D resistance to the lower or higher directions. This function can be interpreted such that the neuron circuit has both excitatory and inhibitory synapses.

3. Feedforward-type Neural Networks

In this section, a two-layered neural network is considered, in which the outputs of m neurons in the first layer are assumed to be fully connected to n neurons in the second layer. This assumption means that each neuron in the second layer has m synapses on it. In the proposed circuits, the m synapses are implemented as parallel connection of AL-FETs. Thus, the synapse array for the second layer is expressed as shown in Fig.3. In this figure, each neuron part corresponds to the circuit enclosed with a broken line in Fig.2 and optical coupling between neurons is assumed.

Layout of the synapse array is shown in Fig.4, in which Si stripes with a lateral npn structure are placed on an insulating substrate and then covered with a uniform ferroelectric film, and metal stripes are placed on the film perpendicular to the Si stripes. In this structure, the Si stripes correspond to the parallel connection of MISFETs, while the metal stripes correspond to the gate electrodes. It is interesting to note that there is no via-hole across the ferroelectric film in the synapse array region. Because of this feature, the packing density of synapses is expected to be very high. For example, when the 1-μm rule is used, the area of each synapse is about 4×2 μm^2 (3-μm-wide Si stripes, 1-μm-wide metal stripes, and 1-μm-wide spaces).

The second feature of this layout is that the Si stripes are electrically isolated from one another. Because of this structure, a pulse bias voltage of $+V_0/2$ and a DC bias voltage of $-V_0/2$, for example, can be applied to the selected metal and Si stripes, respectively, so that the voltage difference V_0 across the ferroelectric film exceeds the critical value for polarization reversal only at the cross point. Since the polarization condition can be adjusted by changing the pulse duration, this method is particularly useful for determining the initial weight of individual synapses.

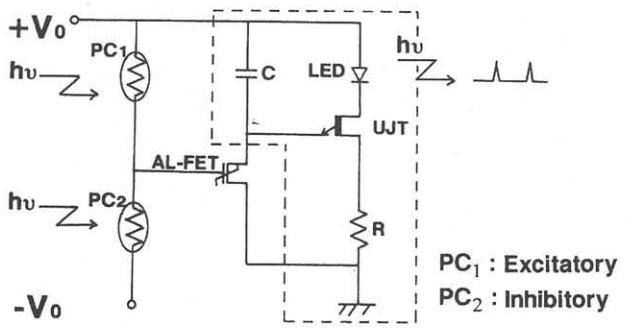

Fig.2.Optically connected neuron circuit with excitatory and inhibitory synapses.

4. Feedback-type Neural Networks

In the feedback-type (Hopfield type) neural networks, the activity of the i-th neuron is described as,

$$\tau_i \frac{du_i}{dt} = -u_i + \sum_j w_{ij} V_j + T_i \qquad (1)$$

$$V_i = g(u_i) \qquad (2)$$

where, τ_i, u_i, V_j, T_i, and w_{ij} are a time constant, the potential level, the output, the threshold value, and the synaptic weight from the j-th neuron to the i-th one[3]. In these equations, the solution $u_i(t)$ is known to settle down to a stable equilibrium value, if g(u) has a saturation nonlinearity and the w_{ij}'s are symmetric. It has also been shown that an analog electrical circuit shown in Fig.5 satisfies these equations.

Here, I attempt to modify the circuit so that each neuron outputs PFM signals (frequency : f_i) and the adaptive learning operation can be conducted. For this purpose, the resistor array in Fig.5 is replaced with the

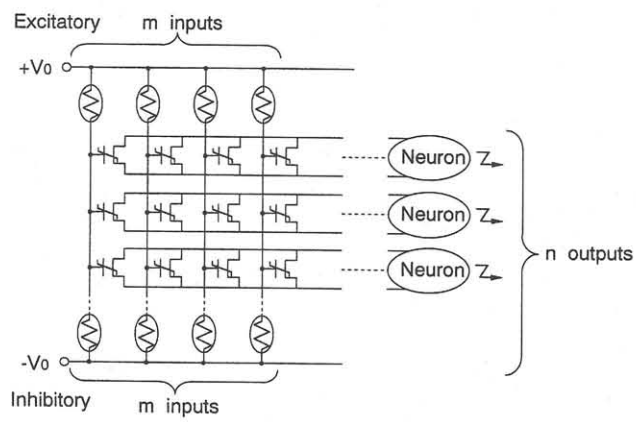

Fig.3. An optically connected multiple-input neuron circuit with m×n synapse array.

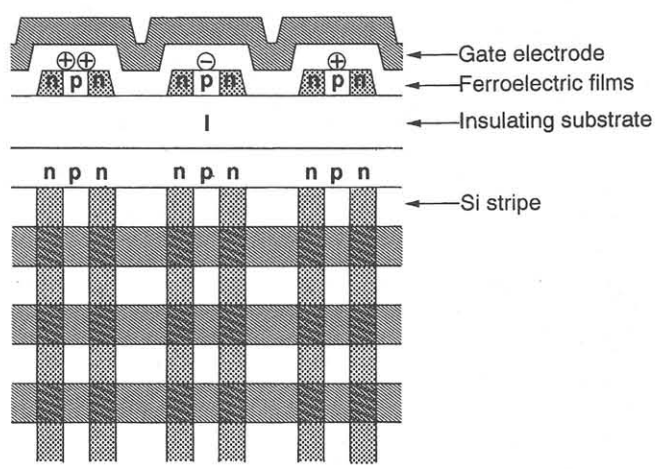

Fig.4. Cross section (top) and top view (bottom) of the synapse array.

FET matrix shown in Fig.3 and the voltage amplifier is replaced with a voltage-to-frequency converter composed of a UJT oscillator. The modified circuit for the i-th neuron is shown in Fig.6. Operation of this circuit is analyzed as follows. First, an FET located at a position (i,j) o follow a constant charge Q_{ij} when a voltage pulse from the j-th neuron is applied to the gate. The assumption that Q_{ij} is independent of u_i is considered to be reasonable, since an FET acts as a constant current source under appropriate bias conditions. Then, the total current flowing into the node A is expressed as $\sum_j Q_{ij}f_j$.

Next, operation of the voltage-to-frequency converter is considered. In this circuit, the capacitance C_i is assumed much larger than C_i' and R_i is also assumed to be a large value. Under these conditions, u_i behaves like a constant voltage source for high frequency current produced by the periodic charging and discharging actions of C_i', but it varies slowly with time by charging and discharging of C_i. It is evident that no output signals are generated, if u_i is lower than the emitter threshold voltage V_T at which the UJT is switched on. This condition corresponds not only to the case where the input pulse frequency f_j is low, but also to the case where C_i is not fully charged.

When u_i exceeds V_T, the charging and discharging actions of C_i' begin and the output signals are generated. The relations among f_i, V_T, u_i, and the average current I_R through R_i can easily be calculated using a simple charging theory of an RC circuit. The results are shown in Eqs.(3) and (4).

$$V_T = u_i[1-\exp\{-1/(R_iC_i'f_i)\}] \qquad (3)$$

$$I_R = C_i'V_Tf_i \qquad (4)$$

The output frequency f_i is derived from Eq.(3) as a function of u_i and it is approximated by Eq.(5), when u_i is much larger than V_T.

$$f_i = (u_i - V_T/2)/(R_iC_i'V_T) \qquad (5)$$

Thus, the following equation holds from Kirchhoff's law at the node A.

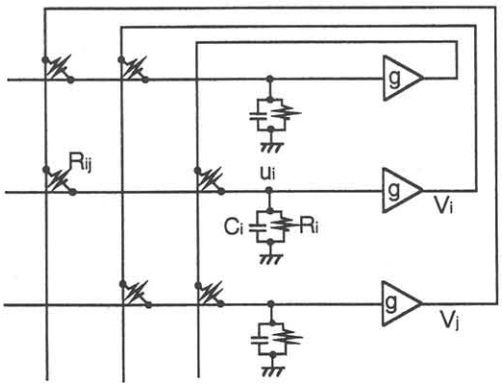

Fig.5. A feedback-type neural network implement by an analog electrical circuit.

$$\sum_j Q_{ij}f_j = C_i\frac{du_i}{dt} + (u_i - \frac{V_T}{2})\frac{1}{R_i} \qquad (6)$$

This equation satisfies the form of Eq.(1), by setting $\tau_i = C_iR_i$. In this analysis, however, the output frequency f_i does not saturate for a large value of, as shown in Eq.(5). This problem will be solved in the actual circuit, since any UJT can not oscillate beyond its maximum frequency.

I conclude from these results that the output frequency f_i of the circuit shown in Fig.6 gives a stable solution of the feedback-type neural network and that the synaptic weights of the network, which are given by the S-D resistance of FETs with ferroelectric gate insulator films, can be modified by adaptive learning.

5. Summary

The circuitry and device structures of the adaptive-learning neural networks were proposed and the stability of the feedback-type network was discussed. New proposals in this presentation are summarized as follows.

1) From a viewpoint of the power consumption, PUTs (programmable unijunction transistors) are considered to be better than UJTs.
2) An adaptive-learning neuron circuit applicable to the feedback-type neural network can be realized using the PFM system, if an additional capacitor is attached to the basic circuit.

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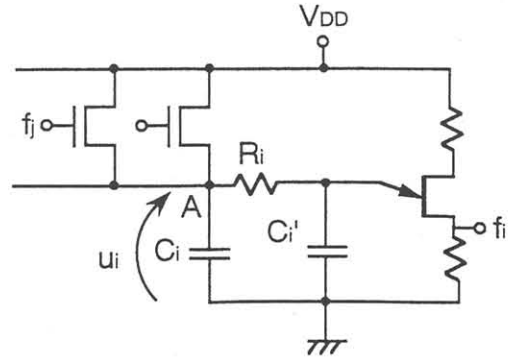

Fig.6. A proposed feedback-type adaptive-learning neuron circuits.