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High-Performance Buried-Gate MOSFETs with RTO-Grown Ultrathin Gate Oxide Films

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We have proposed a novel buried-gate MOSFETs (BG-MOSFETs) with ultrathin gate oxide films formed by rapid thermal oxidation (RTO) technology. The optimized BG-MOSFET enables longer effective channel length, larger avalanche breakdown voltage and much less hot-carrier degradation. Two-dimensional simulation for electric-field and electron density distribution around a trench corner indicates that a muximum electric field is localized near the drain edge, whereas the position of maximum electron density shifts toward the bottom side.

1. INTRODUCTION

Many attempts have been made to realize high speed and high integration MOSLSIs [1]. These attempts focused attention mainly on short channel MOSFETs. However, serious problems such as poor punch-through breakdown characteristics between source and drain, and a large threshold voltage fluctuation caused by channel length modulation effects arise. The former limitation determines the maximum supply voltage of MOSFETs. The latter reduces the noise mergin of the circuits resulting in low reproducibility of the LSI. In previous work, grooved gate MOSFET has been proposed by Nishimatsu et al. [2]. High punch-through breakdown voltage and little threshold voltage fluctuation was realized. However, reliability issue such as transconductance degradation, gate oxide reliablity and guideline for future scaling down still remains. Moreover, it is difficult to form uniformly the gate oxide film on the trench of grooved-type MOSFET structure for obtaining reliable device operation. In recent years, trenches have been mostly studied as a capacitor and an isolation of MOSLSIs [3,4]. The main factors degrading the reliability of trench device are known to be SiO_2 thinning and electric field localization at the corners of trenches. During the oxidation, compressive stress in SiO_2 film causes Si protrusion at convex corners and concave structures reportedly leading to a decrease in SiO_2 film thickness.

In this paper, a scaled and reliable buried-gate-type (BG-MOSFET) with ultrathin gate oxide film formed by rapid thermal oxidation ((RTO) technology [5,6] is proposed for the first time. Two-dimensional numerical analysis of MOSFETs are extended for electric field and electron density distributions in BG-MOSFET channel regime.

2. DEVICE FABRICATION

The BG-MOSFETs were fabricated via the process shown in Fig.1. A schematic drawing of the BG-MOSFET in comparison with planar-type (conventional) is illustrated in Fig.2. Before LOCOS oxidation, B^+ ions were implanted as a channel stopper. The BG-MOSFET fabrication process is as the same as conventional silicon gate technology. However, trench was formed at the gate region by reactive ion etching (RIE) technique using CCl_2F_2 gas and photoresist mask. The resultant trench depth (D) was 0.1-0.5 um in the range. The profile of trenches was optimized by the control of etching gas pressure and RF power condition. In the BG-MOSFETs, channel length (L_M) of the photomask desigh was in the range of 1.0-2.0 um. Junction depth (X_j) was fixed at 0.17 um. Two kind of gate oxide films with 15 nm in thickness were formed using furnace oxidation (FO) in dry oxygen at 950°C, and RTO in dry oxygen at 1100°C. N^+-polysilicon films were deposited as a gate electrodes. In the fabricated BG-MOSFETs, the effective channel length (L_{eff}) is obtained as follows;

$$L_{eff} = L_M + 2.6xD - 0.3 \ (um) \qquad (1)$$

which is determined by S/D resistance, sheet resistance and channel width of the device.

- B^+ ion implantation
- LOCOS isolation
- Trench photo & etching
  D=0.1-0.5 um
- Gate oxidation
  Furnace & RTO 15 nm
- B^+ ion implantation
  V_t control
- Polysilicon/WSi_x deposition
- RIE gate etching
- BPSG deposition/flow/etching
- N^+ source/drain formation
- Al depo/etching
- Al sinter

Fig.1 Process flow for fabrication of a buried-gate MOSFETs.

3. RESULTS & DISCUSSION

Figure 3 shows cross-sectional transmission electron microscope (TEM) images of FO- and RTO-grown oxide films on a convex upper corner of the BG-MOSFETs. No protrusion at the corner is observed, and quite uniform oxide thickness is obtained only for RTO gate BG-MOSFETs. Since RTO is a high temperature process [6], the viscous flow of SiO_2 is thought to relieve convex upper corners from compressive stress, and consequently to suppresses SiO_2 thinning [7]. In addition, RTO has no appreciable negative effect on concave bottom edges. Figure 4 shows cummurative time-dependent dielectric breakdown (TDDB) characteristics for grooved gate 40 MOS capacitors and corresponding planar capacitors. The TDDB data indicate that the breakdown time (T_{BD}) of the RTO oxide film is about 100 times longer than that of FO oxide film, and exactly corresponds to the value of the planar device, as shown in Fig.4. These findings show that RTO rounds off convex upper corners, then electric field localization at corners is relieved.

Then, the 1.0-um-channel BG-MOSFET with RTO oxide film is fabricated. Experimental I_{ds}-V_{ds} characteristics showed that for the planar-type MOSFET, avalanche breakdown (V_{av}) occurs at V_{ds}=6 V, whreas no breakdown is observed in the BG-MOSFET above D=0.2 um, as shown in Fig.5. However, it is noted that with increasing effective channel length (L_{eff}), the I_{ds} itself decreases. In Fig.6, the V_{av}-L_{eff} characteristics indicate that V_{av} above 8 V is obtained when the condition of $D>X_j$ is chosen. Next, hot-carrier trapping behavior is investigated by monitoring substrate current (I_{sub}). The I_{sub} exhibits exponential decay with increasing L_{eff}, as seen in Fig.7. However, dramatic decrease of I_{sub} is obtained under the condition of $D>X_j$, and its dependence is found for various bias conditions. In other words, hot-carrier generation can be avoided in BG-MOSFETs with

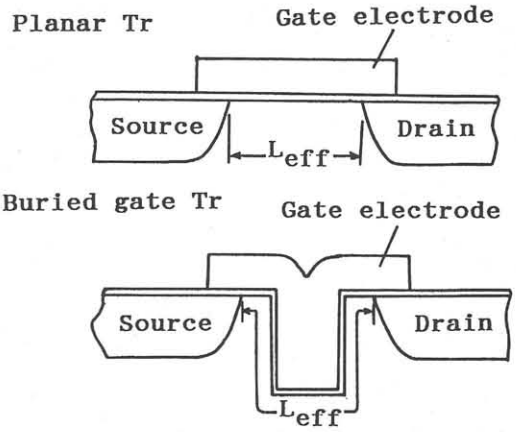

Fig.2 Schematic drawing of planar-type and BG-MOSFETs.

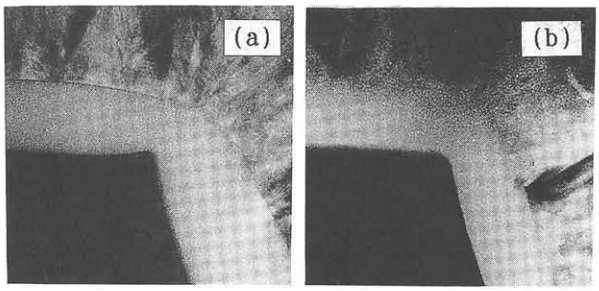

Fig.3 Cross-sectional TEM images of upper edges of BG-MOSFETs. (a) furnace (b) RTO-grown oxide film.

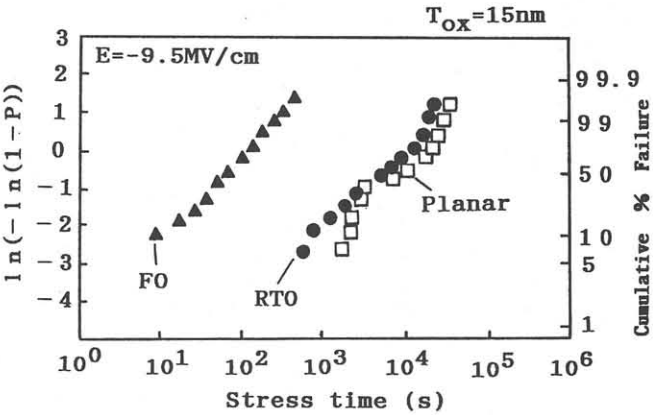

Fig.4 Cumulative TDDB characteristics for BG-type and planar-type MOS devices.

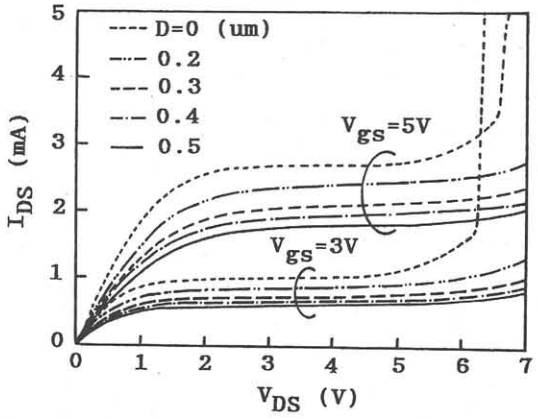

Fig.5 The experimental I_{ds}-V_{ds} of BG-MOSFET with gate length of 1.0 um.

trenchs deeper than X_j. The transconductance (g_m) degradation characteristics showed that the g_m degradation of the BG-MOSFET is much smaller than that of planar-type MOSFETs, as shown in Fig.8. From these results, there is an optimum condition between current gain, avalanche breakdown voltage and hot carrier immunity. That is, the increase of trench depth provides L_{eff} increase, but induces I_{ds} decrease. Thus, it is considered that the optimum trench depth is deeper about 0.1-0.2 um than junction depth.

Two-dimensional simulation for electric-field and electron density distribution around a trench corner indicates that a maximum electric-field is localized near the drain side and is not dependent on the trench depth, as shown in Fig.9. On the contrary, the position of maximum electron density shifts toward the bottom side (Fig.10), depending on the trench depth. Thus, it is suggested that the channel is usually formed on the deeper side, and the hot-carrier generation rate then becomes much smaller as compared to that of planar-type MOSFETs.

4. CONCLUSION

A novel buried-gate-type MOSFET was proposed. The device showed high punchthrough characteristics and much less hot-carrier degradation. The optimum trench depth is about 0.1-0.2 um deeper than junction depth considering current gain, avalanche breakdown voltage and hot-carrier immunity.

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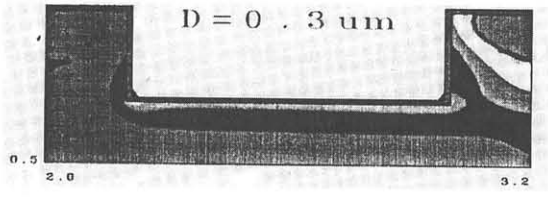

Fig.9 Two-dimensional simulation of electric-field of BG-MOSFETs.

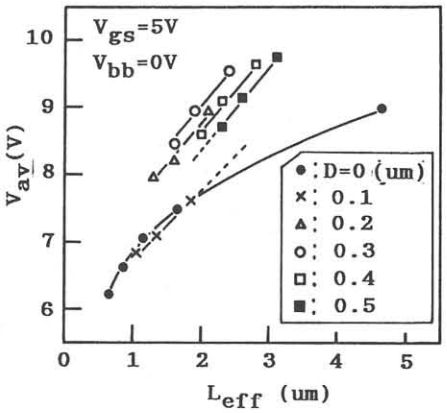

Fig.6 The V_{av}-L_{eff} characteristics as a function of trench depth.

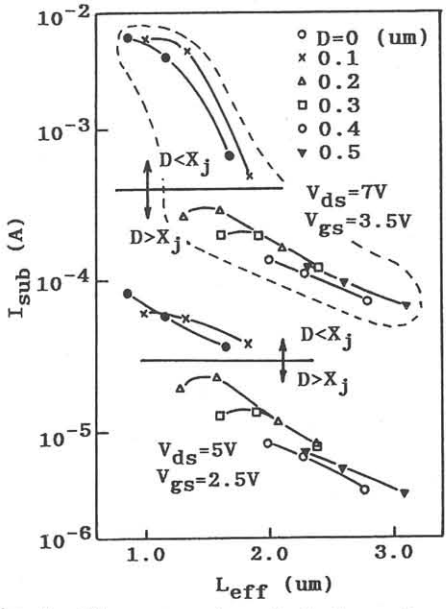

Fig.7 The experimental I_{sub}-L_{eff} characteristics of BG-MOSFETs.

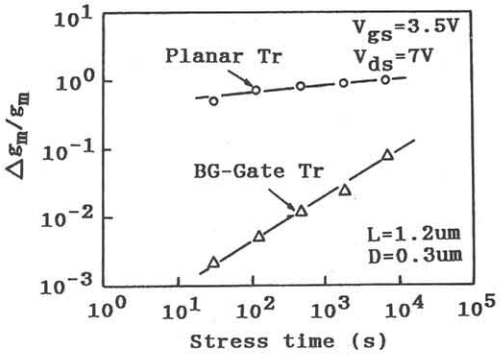

Fig.8 The $\Delta g_m/g_m$ characteristics for planar and BG-MOSFETs.

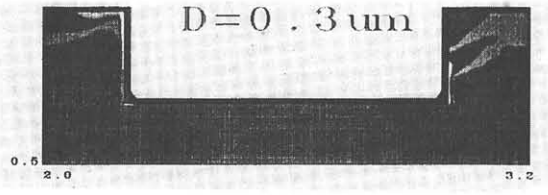

Fig.10 Two-dimensional simulation of electron density of BG-MOSFETs.