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Structure and Characteristics of 0.1μm to sub-0.1μm Devices

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The device structure and the device design methodology to achieve the sub-0.1um MOS transistors are discussed. It is shown in the simulation that it is difficult to simultaneously satisfy the requirements to suppress the short channel effect and to improve the device performance in the sub-0.1um devices. In order to experimentally evaluate this, the sub-0.1um devices with the gate length of 0.07um was fabricated. It is demonstrated that the short channel effect can be sufficiently suppressed by employing the double punchthrough stopper structure (DPT) even in the 0.07um MOSFET although the current drivability was not improved so much. The conduction mechanism in such small devices was also discussed.

1. Introduction

The feature size of MOSFET has been rapidly reduced according to the scaling-down rule. It has been so far the most important issue for scaling-down the device size to guarantee the hot carrier reliability. In the 0.1um and sub-0.1um regime, however, to suppress the short channel effect and the source-drain punchthrough is the most crucial issue[1]. The active power and stand-by power for the device operation can be reduced by lowering the supply voltage and suppressing the short channel effect and the punchthrough. The reduction of the noise margin by lowering the supply voltage can be compensated by improving the device performance. Therefore, the low-voltage and low-power operation of sub-0.1um devices becomes possible if it can be simultaneously realized to suppress the short channel effect and to improve the device performance. However, it is not so easy to simultaneously satisfy these two requirements because they are contradictory each other.

In this paper, it is discussed whether these requirements can be simultaneously satisfied in the bulk MOSFET with sub-0.1um size.

2. Design of Sub-0.1um MOSFET

The conditions to suppress the short channel effect and to improve the device performance in the sub-0.1um devices are examined using the two-dimensional device simulator with hydrodynamic model. The device used in the simulation is the double punchthrough stopper (DPT) transistor. The simulated results for the saturation-region threshold voltage vs. gate length relation are shown in Fig.1 where the peak impurity concentration in the n^- LDD region is changed as a parameter. The gate oxide thickness, the n^- junction depth, the n^+ junction depth and the side-wall spacer length are 4nm, 40nm, 80nm and 0.1um, respectively. The peak concentration and depth of the substrate punchthrough stopper are $2\times10^{18}cm^{-3}$ and 0.074um, respectively. The threshold voltage vs. gate length relation is improved with decreasing the n^- impurity concentration. It is obvious in the figure that the n^- impurity concentration should be decreased to less than $5.0\times10^{18}cm^{-3}$ to suppress the punchthrough in the device with the gate length of 0.07um although $1\times10^{19}cm^{-3}$ is acceptable for the 0.1um device. However, such low n^- impurity concentration results in the reduced current drivability. Figure 2 shows the simulated drain current-voltage characteristics. The drain current at V_D=1V is reduced to one half when the n^- impurity concentration is decreased from $1\times10^{19}cm^{-3}$ to $5.0\times10^{18}cm^{-3}$. Thus, it is no longer possible to simultaneously satisfy two requirements to suppress the shortchannel effect and to improve the current drivability in the sub-0.1um devices.

The electric field distribution and the electron temperature distribution near the drain are depicted in Fig.3. The horizontal electric field along the channel near the drain increases with increasing the n^- impurity concentration while the electron temperature less significantly increases with the n^- impurity concentration. This implies that electrons can not sufficiently gain the energy from the rapidly changing electric field along the channel direction when the electric field is high. Therefore, the hot carrier effect becomes less serious in the sub-0.1um devices although it is not neglected.

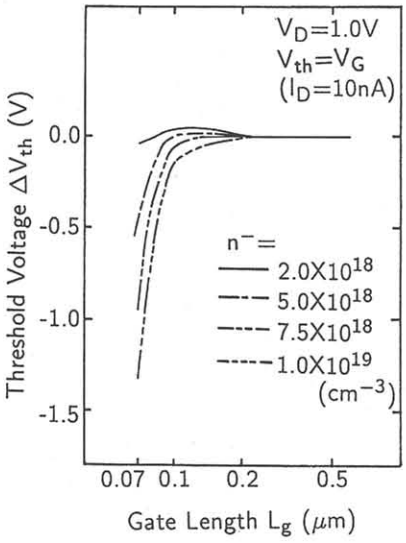

Fig.1 Simulated gate length dependence of threshold voltage.

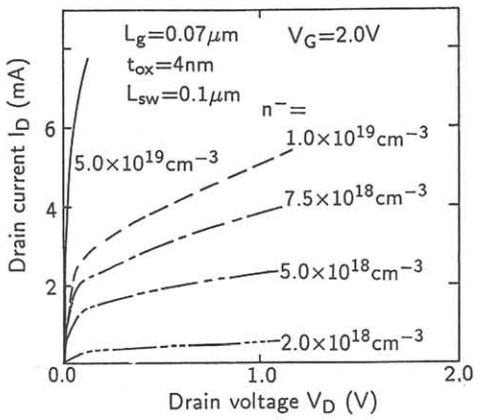

Fig.2 Simulated I_D-V_D characteristics of DPT MOSFET.

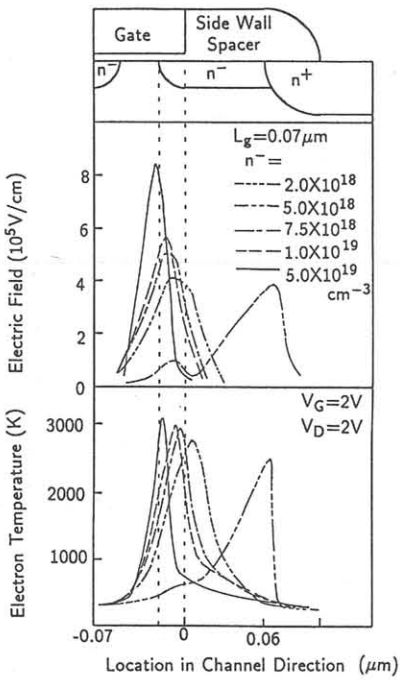

Fig.3 Electric field and electron temperature distributions.

3. Sub-0.1um Device Fabrication and Evaluation

The sub-0.1um bulk MOSFET with the gate length of 0.07um was fabricated and evaluated in order to confirm the discussions in the previous section. The cross-sectional view and SEM cross-section of the fabricated DPT MOSFET with L_G= 0.07um are shown in Fig.4. The I_D-V_D characteristics of this device are shown in Fig.5. It is clear that the 0.07um DPT MOSFET successfully operates with the excellent cut-off behavior even at 3V supply voltage as a result of suppressing the short channel effect. The cut-off current at V_G= 0V was around 1 pA at V_D= 3V. Fig.6 shows the L_G dependence of the saturation region threshold voltage Vth. The excellent Vth-L_G relation was obtained with channel implant dose of $2\times10^{12}cm^{-2}$ and 140KeV implanted punchthrough stopper although the reverse short channel effect is observed. The gate length dependence of the linear region transconductance g_m is shown in Fig.7. The transconductance increases with decreasing the gate length. However, the value of g_m is not so large due to the relatively low n^- impurity concentration. Thus, it is difficult to simultaneously satisfy two requirements to suppress the short channel effect and to improve the device performance in the sub-0.1um devices. As for the hot carrier reliability, it was obtained that the supply voltage to guarantee the 10 year life time in the 0.07um devices is 1.7V[2),3)].

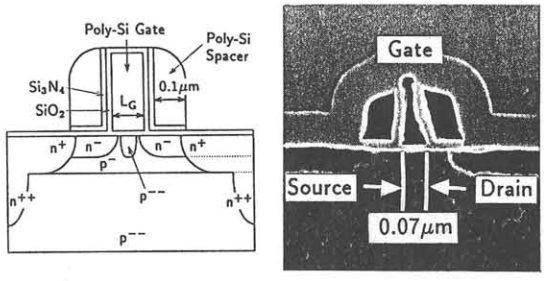

Fig.4 SEM cross-section of DPT MOSFET.

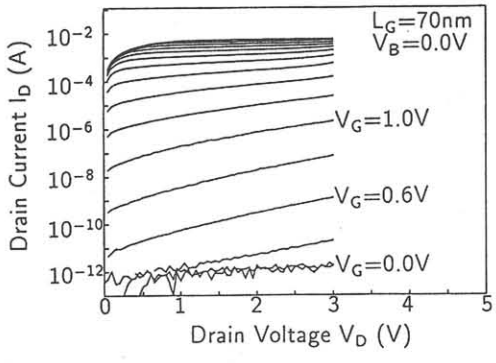

Fig.5 I_D-V_D characteristics.

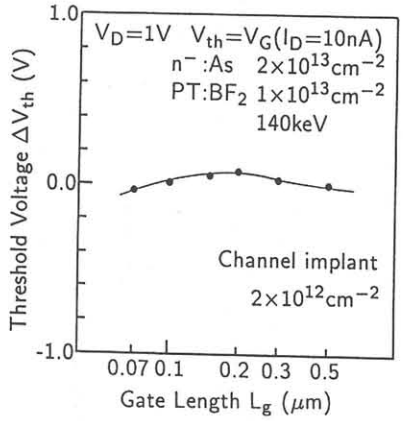

Fig.6 Gate length dependence of threshold voltage.

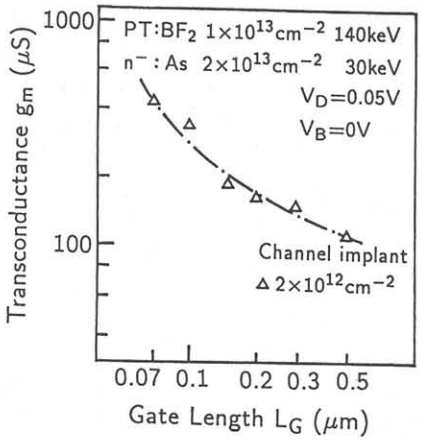

Fig.7 Gate length dependence of transconductance.

4. Velocity Overshoot and Impact Ionization

The device performance can be improved more by reducing the gate length if the relatively large off-current is permitted because the velocity overshoot effect becomes significant. The electron population in the conduction band, the electric field distribution, the electron temperature distribution and the electron drift velocity distribution obtained from the Monte Carlo simulation are plotted in Fig.8. As is obvious in the figure, the drift velocity of electrons exceeds the saturation velocity in the whole channel region when the gate length is reduced. Therefore, it can be expected that the current drivability is still improved by reducing the device size even in the sub-0.1um regime if it is allowed to pay the penalty of the larger off-current. Thus, the drift velocity can be increased beyond the saturation velocity in the sub-0.1um devices while the carrier energy can not increase so much. As a result, the impact ionization probability decreases as the gate length is reduced to sub-0.1um regime. On the contrary, however, the impact ionization can occur at the low drain voltage of less than 1.1V as shown in Fig.9.

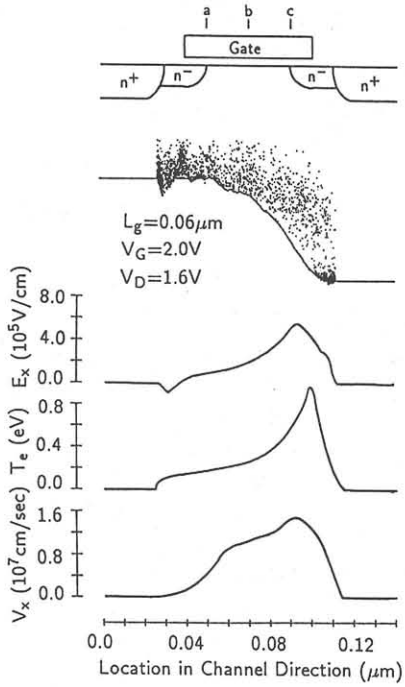

Fig.8 Electron population, electric field, electron temperature and drift velocity distributions obtained by Monte Carlo simulation.

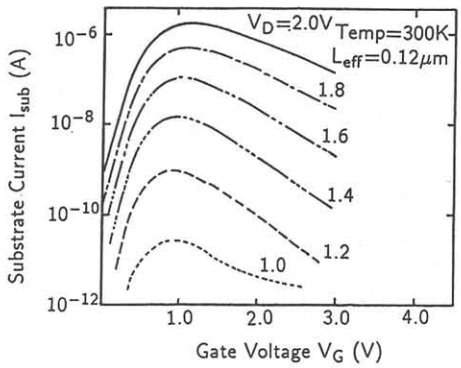

Fig.9 Gate voltage dependence of substrate current changing the drain voltage as a parameter.

5. Summary

The double punchthrough stopper MOS transistor was examined for achieving the sub-0.1um devices. It was revealed by the simulation and the experiment that it is difficult to simultaneously satisfy two requirements to suppress the short channel effect and to improve the device performance in the sub-0.1um regime even though the double punchthrough stopper structure is employed.

References

1) T. Hashimoto et al., Ext. Abs. of Int. Conf. Solid State Devices and Materials, p.490 (1992)
2) M. Koyanagi et al., IEDM Tech. Dig., p.1019 (1992)
3) H. Kurino et al., IEDM Tech. Dig., p.1015 (1992)