Extended Abstracts of the 1993 International Conference on Solid State Devices and Materials, Makuhari, 1993, pp. 23-25

Significance of Charge Sharing in Causing Threshold Voltage Roll-Off in Highly Doped 0.1-μm Si MOSFETs and Its Suppression by Atomic Layer Doping(ALD)

Hiromasa Noda, Kaori Nakamura, and Shin'ichiro Kimura

Central Research Laboratory, Hitachi Ltd.
1-280, Higashi-koigakubo, Kokubunji-shi, Tokyo 185, Japan

Abstract **- An investigation of the influence of substrate dopant concentration on the short channel effects in 0.1-μm nMOSFETs shows that threshold voltage roll-off is not suppressed by heavy doping and that there is a clear reduction in subthreshold swing at dopant concentrations higher than 1×10^{18} cm^{-3}. These results can be explained by the charge sharing concept and, we demonstrate the excellent scalability of the ALD (atomic-layer doped) MOSFET, in which the charge sharing can be effectively suppressed.**

1. Introduction

Recently several 0.1-μm MOSFETs have been fabricated and their excellent performance was demonstrated [1-3]. However, threshold voltage (*Vth*) roll-off was not suppressed satisfactorily, even though their substrate dopant concentration, profile, and junction depth were adequate. This paper intensively investigates the influence of substrate dopant concentration on the short channel effect (SCE), and demonstrates that heavy doping does not suppress *Vth* roll-off. These results can be explained by the charge sharing concept [4]. The charge sharing can be effectively suppressed in an ALD (Atomic Layer Doped) MOSFET [5], which has a stepped dopant profile.

2. Dependence of short channel effects on dopant concentration

Single-drain n-channel MOSFETs were fabricated with various dopant concentrations whose peak is located around the source/drain junction (0.1 μm). Figure 1 shows the channel length (*Leff*) dependence of *Vth*, subthreshold swing (*S*), and leakage current (*Ileak*) at the flat band condition. Two kinds of minimum channel length are defined as parameters for evaluating the extent to which SCE is suppressed. L_{min}^{RO} is the channel length where $\Delta Vth / \Delta Leff = 0.1$ V / 0.1 μm, indicating the beginning of *Vth* roll-off. L_{min}^{PT} is the channel length where $Ileak = 0.1$ pA, indicating punchthrough.

For the lower peak concentration case of 6.0×10^{16}

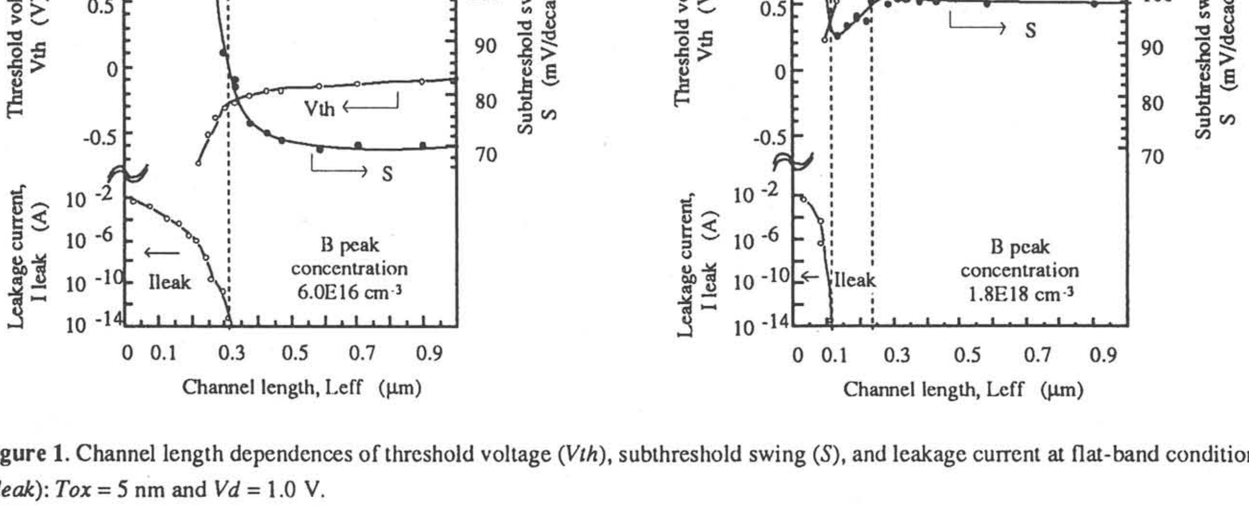


Figure 1. Channel length dependences of threshold voltage (*Vth*), subthreshold swing (*S*), and leakage current at flat-band condition (*Ileak*): *Tox* = 5 nm and *Vd* = 1.0 V.

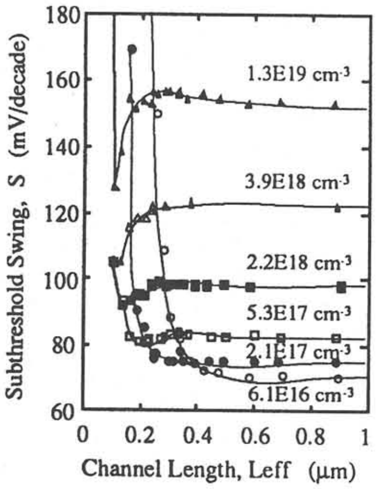


Figure 2. Dependence of S on dopant concentration : Vd = 1.0 V.

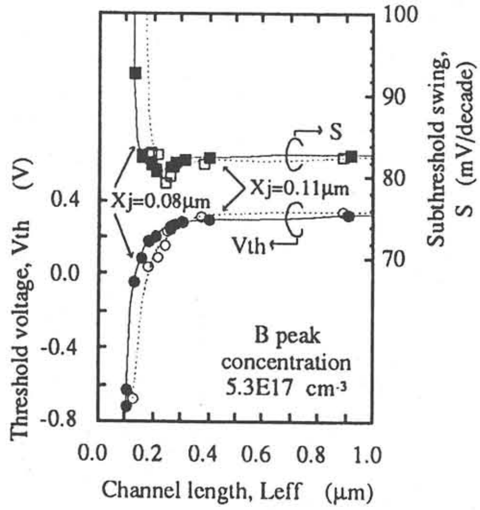


Figure 3. Dependence of Vth and S on junction depth : Vd = 1.5 V.

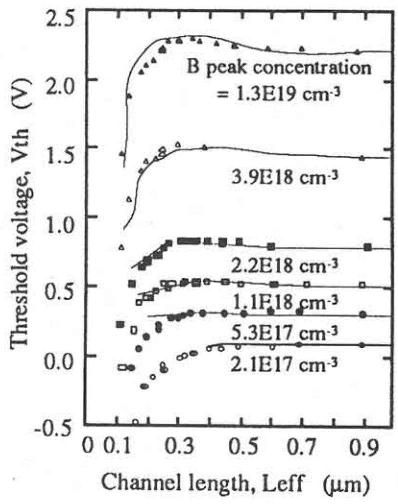


Figure 4. Channel length dependence of Vth.

cm^{-3} (a), L_{min}^{RO} and L_{min}^{PT} are identical. In contrast, for the higher concentration case of 1.8×10^{18} cm^{-3}(b), L_{min}^{RO} is no longer identical to L_{min}^{PT}. In addition, it is found that Vth roll-off is accompanied by a reduction in S for case (b).

The dependence of S on dopant concentration is shown in Figure 2. The reduction in S is amplified as the dopant concentration increases. Figure 3 shows the dependence of Vth and S on junction depth. Vth roll-off and S reduction are suppressed as the junction depth becomes shallow.

These results strongly suggest that the two-dimensional shape of the drain depletion region is the dominant factor in SCE. In other words, the charge sharing concept [4] needs to be reconsidered.

Assuming that the reduction in S is attributed to the decrease in channel space charge caused by the drain electric field, the charge sharing factor f is obtained from the following formula.

$$S = kT/q \ln 10 (1 + f\, Cd / Cox),$$

where Cd is the depletion capacitance and Cox is the oxide capacitance. Then Vth is calculated using the following formula,

$$Vth = Vfb + 2\,\phi s + f\, Qd / Cox,$$

where Vfb is the flat-band voltage, ϕs is the potential difference between the Fermi level and the intrinsic Fermi level of the bulk, and Qd is the depletion charge. Figure 4 shows that excellent agreement between the measured Vth (points) and the calculated Vth (solid-lines) is obtained, especially at higher concentrations exceeding 1.0×10^{18} cm^{-3}. The absence of the calculated Vth at the short channel region of the lightly doped MOSFETs is attributed to punchthrough, which makes this model invalid.

The influence of heavy doping on SCE is summarized in Figure 5. It is demonstrated that heavy doping in the substrate works effectively to suppress punchthrough. However Vth roll-off is found not to be suppressed by heavy doping.

These results described in this chapter indicate the significance of the charge sharing. Therefore, Vth-controlled sub-0.1 μm MOSFETs will require a new approach to suppressing the charge sharing.

3. Suppression of charge sharing by atomic-layer doping (ALD)

One candidate which has immunity to the charge sharing is the ALD MOSFET [5]. In this section, the excellent scalability of the ALD MOSFET, which has a stepped dopant profile, is discussed based on device simulation from the viewpoint of charge sharing .

Three doping profiles were used for comparison as shown in Figure 6. For the ALD MOSFETs (b and c), step functions were used as the ideal case. The channel length dependences of Vth and S are shown in Figure 7. There is no reduction in S for the ALD MOSFET, which indicates that the charge sharing is suppressed, resulting in good short channel behavior. Furthermore, a lower

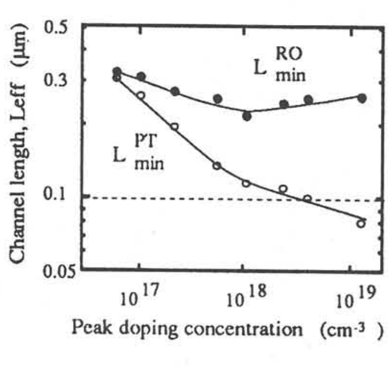
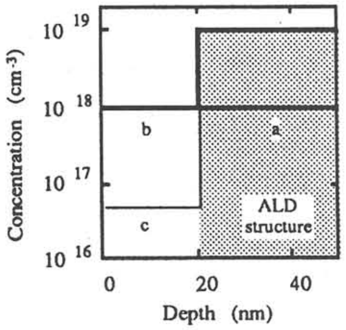


Figure 5. Dependence of the two minimum channel lengths on dopant concentration.



a: uniform doping: 1.0E18 cm-3
b: surface: 1.0E18 cm-3: ALD structure: 1.0E19 cm-3
c: surface: 5.0E16 cm-3: ALD structure: 1.0E19 cm-3

Figure 6. Doping profiles used for the simulation.

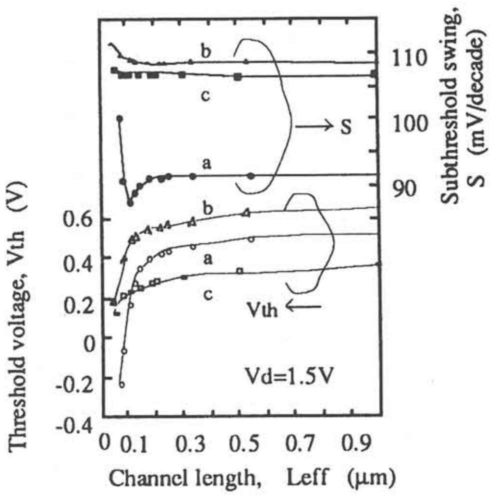


Figure 7. Channel length dependence of *Vth* and *S* of the three MOSFETs (*a*, *b*, and *c*).

surface dopant concentration leads to better short channel behavior. The minimum L_{min}^{RO} was found to be 0.07 μm by simulation.

Two-dimensional potential plots of long-channel devices corresponding to the three cases are shown in Figure 8. The shaded region is the drain depletion region determined from the electric field lines which terminate on the drain [6]. The darker shaded region is the extended area of the drain depletion region to the channel area. This extended area is bounded by the horizontal line tangent to the channel depletion edge, the line perpendicular to the gate and the curved drain edge. The expansion of this region causes the charge sharing. In comparison with the uniformly doped device (*a*), the ALD structure (*b*) effectively suppresses the expansion. Furthermore, a lower surface dopant concentration (*c*) causes this region to disappear, probably due to the extension of the hooked drain to the channel region.

4. Summary

We have demonstrated the significance of charge sharing, in particular for highly doped devices, as the cause of *Vth* roll-off and *S* reduction. For *Vth*-controlled 0.1-μm Si MOSFETs, suppression of the charge sharing is indispensable, and the ALD MOSFETs are expected to survive device miniaturization down to 0.07 μm with optimized ALD location and low surface concentration.

Acknowledgement

The authors wish to thank Dr. E. Takeda and Dr. T. Toyabe for their helpful discussions and encouragement. Special thanks are due to T. Nishida and the members of the Process Integration Center for device fabrication.

References

[1] R.H. Yan et al., Symp. on VLSI Tech., 86 (1992).
[2] A. Toriumi et al., Ext. Abs. SSDM, 487 (1992).
[3] T. Hasimoto et al., ibid., 490 (1992).
[4] L.D. Yau, Solid-State Electronics, 17, 1059 (1974).
[5] K. Nakagawa et al., Appl. Phys. Lett., 54, 1869, (1989).
[6] C.R. Viswanathan et al., IEEE Trans. Electron Devices, ED-32, 932, (1985).

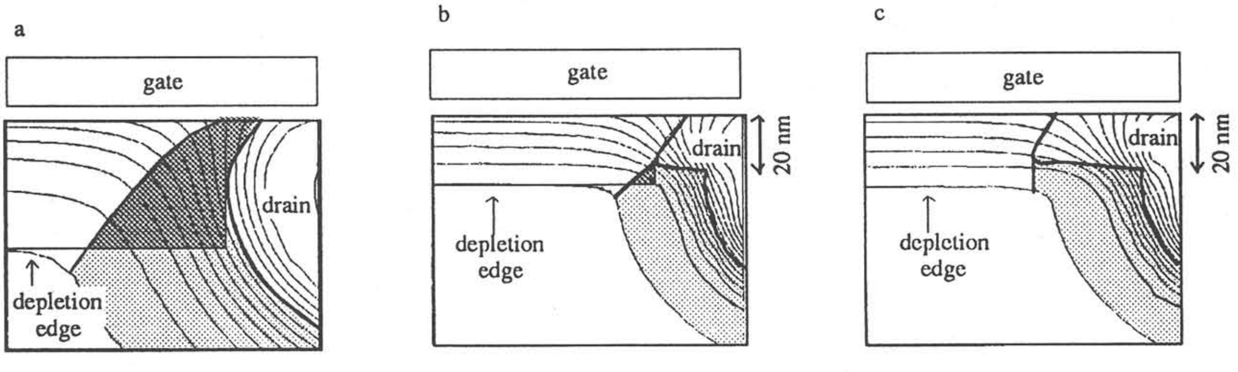


Figure 8. Two-dimensional potential plots for the three cases indicated in Figs. 6 and 7 (*a*, *b*, and *c*). The drain voltage is 1.5 V and gate voltages are set to be *Vth*. The equipotential contours are plotted with an interval of 0.2 V. For the ALD MOSFETs (*b* and *c*), a hooked boundary of drain is formed as a result of low surface concentration.