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Sub 0.1μm nMOSFET Utilizing Narrow Trench Gate and Selective Excimer Laser Annealing (SELA)

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Abstract

Fine n-type MOSFETs with sub 0.1 μm gate length were realized utilizing narrow trench and selective excimer laser annealing (SELA) techniques. Fine gates were formed by filling of narrow trenches with doped poly Si and WSi material. SELA was carried out by adjusting thickness of SiO_2 film, i.e. forming high reflective films on gates for preventing the influence of high energy laser irradiation and low reflective films on source and drain for being annealed effectively. A steep subthreshold slope of 78.6 mV/dec. over 7 decades and less short channel effect on the sub 0.1 μm gate nMOSFET clearly show that SELA is very promising for sub 0.1 μm era.

1. Introduction

In fine gate MOSFETs, prevention of dopant side diffusion is an extremely important technique to keep the effective channel length and to obtain a steep subthreshold slope. Some important factors to obtain the effective channel length are the condition of lightly doped drain (LDD) formation by ion-implantation and the annealing technique, respectively. In LDD formation, it is required to consider the transverse distribution of the dopants, because a ratio of the transverse straggle to the projected range in low energy implantation becomes to be larger than 40 %. On the other hand, the annealing technique needs sufficient dopants activation and control of its side diffusion. Excimer laser annealing (ELA) is one of the promising techniques for this purpose, which has feasibility to suppress the dopant diffusion because of its extremely rapid heating within a few ten nanoseconds [1]. During annealing, however, temperature of the electrodes is estimated to be higher than that of source/drain region because the gate electrodes are thermally isolated from the silicon substrate by the gate oxide films due to the small thermal conductivity [2]. It is necessary to control the overheating of gates for the prevention of fine gate deformation due to the thermal stress. In this paper, temperature transition at gate surface and source/drain during ELA were simulated and fine n-type MOSFETs with sub 0.1 μm gate were fabricated utilizing narrow trench and selective ELA (SELA) techniques to investigate the advantages of ELA for fine MOSFETs.

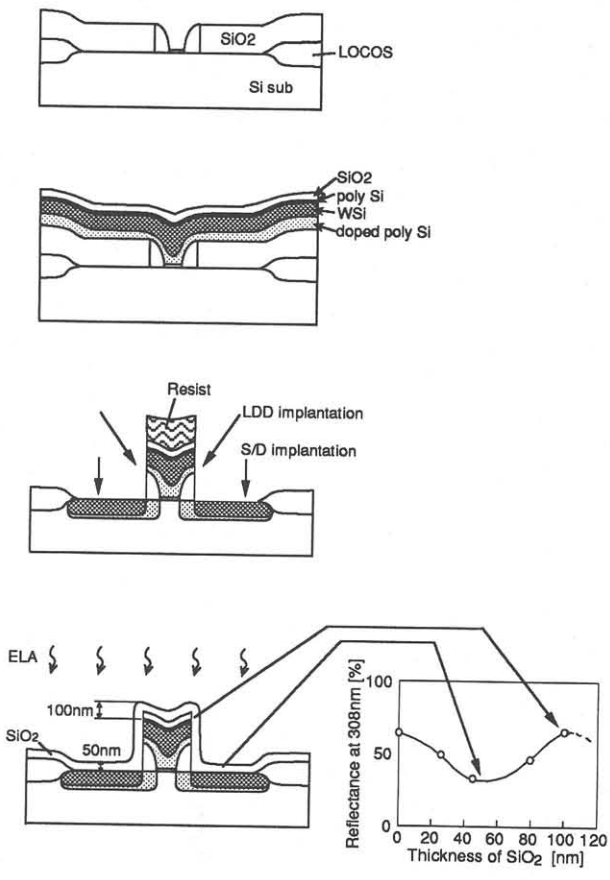
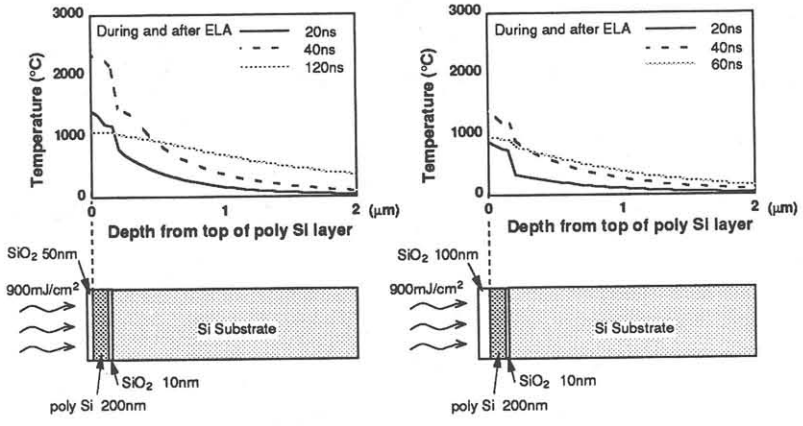


Fig. 1 Process sequence of fine gate MOSFET utilizing narrow trench and selective excimer laser annealing techniques.



(a) Conventional gate structure (b) Improved gate structure

Fig. 2 Temperature distribution and device structures for the simulation .

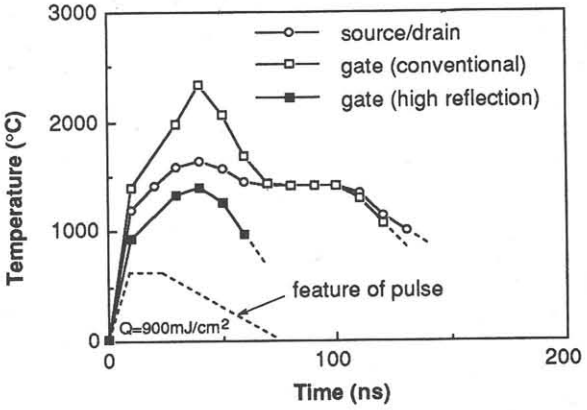


Fig. 3 Simulated temperature transition of sample surface.

2. Device Fabrication

Fig. 1 shows the process sequence for fine gate nMOSFETs utilizing SELA. Side wall spacer of SiO_2 inside the trenches were utilized to reduce gate length [3]. P-type (100) silicon substrates with resistivity of 1 Ωcm were used for this experiment. LOCOS isolation was formed first, followed by deposition of SiO_2 film of 200 nm. Gate trenches with a depth of 200 nm were formed through the SiO_2 film by using negative photoresist and reactive ion etching technique. Boron ions were implanted with a dose of $2x10^{12}$ at 15 keV for adjusting the threshold voltage, and with a dose of $4x10^{12}$ at 60 keV for punchthrough stopper, respectively. These trenches were narrowed by 120 nm SiO_2 side wall spacers. After measuring gate length with SEM, gate oxide films of 8 nm were formed. Doped poly silicon of 100 nm and WSi of 100 nm were deposited to fill the narrowed trenches. Subsequently poly Si of 20 nm was deposited to prevent WSi from barking, followed by SiO_2 of 50 nm deposition to lower reflection. The gates were patterned by a lithographic step using the same gate mask with positive photoresist. After thermal activation of the n^+ doped poly gate region at 1050 °C for 10 s, the deep n^- lightly doped region was formed by P^+ oblique implantation at a dose of $5x10^{12}$ cm^{-2} and an energy of 90keV for obtaining a steep subthreshold slope. The n^+ junction formation was carried out by As^+ implantation with a dose of $3x10^{15}$ cm^{-2} and an energy of 15 keV, followed by SiO_2 deposition of 50 nm over the samples. As a result, SiO_2 films of 100 nm on the gates with high reflectance of 70 % for the excimer laser light with a wavelength of 308 nm and that of 50 nm on source/drain with a low reflectance of 30 % were formed. Preliminary low temperature annealing of 600 °C for 1 h was carried out to reduce the junction leakage current without dopant diffusion [4], followed by single pulse ELA of 850 mJ/cm^2 by step and repeat irradiation over the samples with a uniform energy beam of spot size 5x5 mm^2 using homogenizer. Passivation, opening contact holes and aluminum metallization with TiON/Ti films finalized the processing.

3. Results and Discussion

Typical temperature profiles of samples from the top of poly Si gate to substrate during ELA of 900 mJ/cm^2 are shown in Fig. 2. The simulation is based on a simplified one-dimensional model, which means gate material and silicon substrate have the same specific heat and thermal conductivity, and which also considers the temperature dependence of the characteristics for SiO_2 and for silicon, respectively. A normal gate structure with the low reflective film of 30 % reflectance is represented in Fig. 2(a), which shows that the heat of gate is accumulated on the gate oxide film. Fig. 2(b) shows the case of SELA, the rising of the temperature is remarkably suppressed by the high reflective film of 70 % reflectance. Temperature transition at gate surface and source/drain during ELA of 900 mJ/cm^2 are plotted in Fig. 3. In case of normal gate without the high reflective film, the temperature at top of gate is estimated to be above 2000 °C due to the thermally isolation of gate oxide, which destroys the fine patterned gate. On the other hand, the temperature of gate is limited below the melting point of 1410 °C by the high reflective film of SiO_2 of 100 nm on the gate and normal features of the fine gates are obtained [2]. In case of the source/drain, the temperature at silicon surface is estimated to be higher than the melting point for 100 nanoseconds, which means the activation of source/drain without dopant diffusion is possible. As a result selective ELA (SELA) is proved to be feasible. Id-Vg and Id-Vd characteristics of a sub 0.1 μm gate

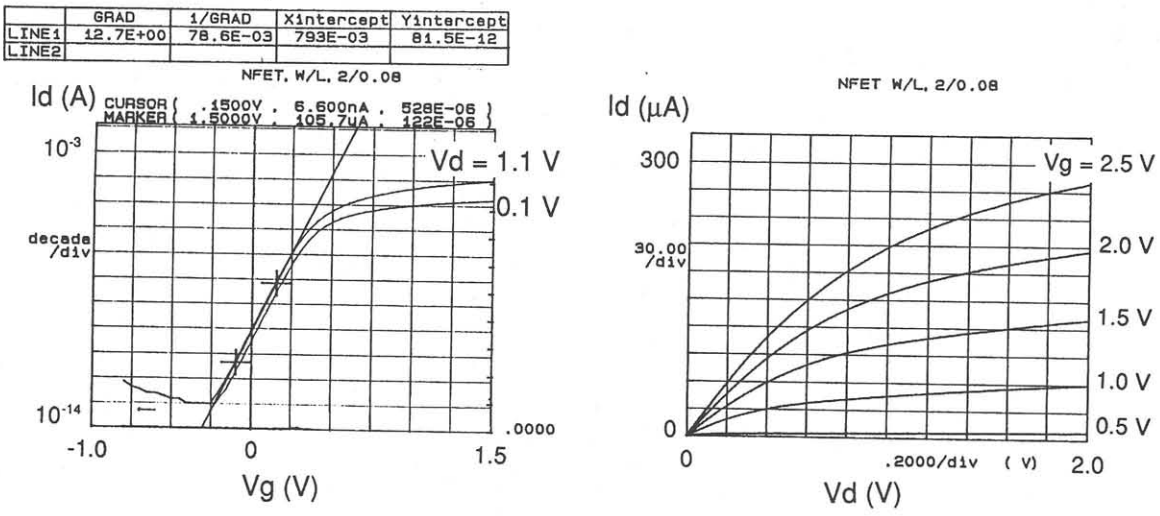


Fig. 4 Typical log Id-Vg and Id-Vd characteristics of 0.08 μm gate nMOSFET (gate W = 2 μm) utilizing selective ELA.

nMOSFET with 2 μm width utilizing narrow trench gate and SELA are shown in Fig. 4. The gate length is estimated to be 0.08 μm by top view SEM measurement of the trench. A steep subthreshold slope of 78.6 mV/dec. with very low leakage current is obtained, which implies reduction of short channel effect. This can be explained by suppression of dopant side diffusion through SELA technology.

4. Conclusion

A steep subthreshold slope of 78.6 mV/dec. over 7 decades was obtained and short channel effect was suppressed on the sub 0.1 μm gate nMOSFET fabricated utilizing narrow trench and selective excimer laser annealing (SELA) techniques. SELA is very promising to overcome serious effects of dopant diffusion on sub 0.1 μm MOSFETs through its extremely short time annealing.

5. Acknowledgements

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6. References

[1] H. Tsukamoto et al., Jpn. J. Appl. Phys., Vol. 31(1992) L659.

[2] H. Tsukamoto et al., Jpn. J. Appl. Phys., to be published.

[3] S. Kimura et al., Tech. Dig. IEDM 1991, p950.

[4] H. Tsukamoto et al., Extended Abstracts (The 40th Spring Meeting, 1993); The Jpn Soc. of Appl. Phys. and Related Societies, p738.