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# Impact of Contact Resistance and Junction Capacitance on the Switching Performance in Scaled 0.1$\mu$m CMOS Devices

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In this paper, the switching performance of scaled 0.10 $\mu$m CMOS devices is discussed on the basis of both experimental and simulated results of 0.10 $\mu$m gate length CMOS devices operating at room temperature. In a fully scaled 0.10 $\mu$m CMOS device, it has been found that optimizing the parasitic effects reduces the propagation delay time $\tau_{pd}$ to less than 20 psec and the power-delay product to less than 10 fJ. However if the specific contact resistance $\rho_c$ will not be reduced to less than $1\times10^{-7}\Omega\text{cm}^2$, the propagation delay time of the fully scaled 0.1 $\mu$m CMOS devices will not be further improved than that of partially scaled 0.1 $\mu$m CMOS devices.

## 1 Introduction

Recently, several studies on 0.1 $\mu$m gate length MOSFETs have been reported [1, 2]. The authors first demonstrated the performance of 0.10 $\mu$m gate length CMOS devices experimentally [3], where it has been found that the parasitic resistance and parasitic capacitance significantly contribute to the total propagation delay time($\tau_{pd}$). This fact means that a quantitative analysis of the propagation delay time taking account of the parasitic effects is strongly needed to expect such actual switching performance in a 0.1 $\mu$m CMOS device with no relevance to process technology employed in device fabrication. This paper gives the results of quantitative discussion on the source/drain junction capacitance effect and the contact resistance effect on the switching performance in scaled 0.1 $\mu$m CMOS devices on the basis of experimental and simulated results of 0.1 $\mu$m gate length CMOS devices. Then, it will be shown that $\tau_{pd}$ in fully scaled down 0.1 $\mu$m CMOS devices would be degraded than that in partially scaled down 0.1 $\mu$m CMOS devices under a fixed $V_{DD}$ in the case of employing a specific contact resistance currently used.

## 2 Junction Capacitance Effect on 0.1 $\mu$m Gate Length CMOS Devices

The switching performance of a 0.1 $\mu$m gate length CMOS device was investigated for the same type of device reported in Reference[3]. These devices were partially scaled devices, and the device width, source/drain junction area, and contact size were not scaled to the 0.1 $\mu$m level. The propagation delay time $\tau_{pd}$ and the power dissipation were measured for the 101-stage ring oscillators (F/O=1) at room temperature. The propagation delay time $\tau_{pd}$ was about 40 psec/stage at 2.5 V in the used standard type ring oscillator because of relatively large parasitic effects such as the junction capacitance ($C_j$) effect. Ring oscillators which had different drain junction areas were fabricated to investigate the $C_j$ effect on $\tau_{pd}$. Figure 1 shows the experimentally measured drain junction area dependence of $\tau_{pd}$ in the 0.1 $\mu$m CMOS ring oscillator. The drain area of the NMOSFETs in the measured ring oscillators were 3.8 $\mu\text{m}^2$, 8.0 $\mu\text{m}^2$ and 16.0 $\mu\text{m}^2$, respectively. The drain area of the PMOSFETs were 1.5 times larger than that of NMOSFETs. A linear relationship between the junction area and $\tau_{pd}$ is found in Fig.1. This clearly demonstrates that a critical consideration for both the junction area and the impurity concentration beneath the source/drain diffusion layer are required to reduce $C_j$ and to achieve higher switching performance.

Next, the power-delay relationships of the 0.1 $\mu$m gate length CMOS devices are shown in Fig.2. The power dissipation is defined as the product of the applied voltage and the total current flow into the ring oscillator, and was measured in the range of

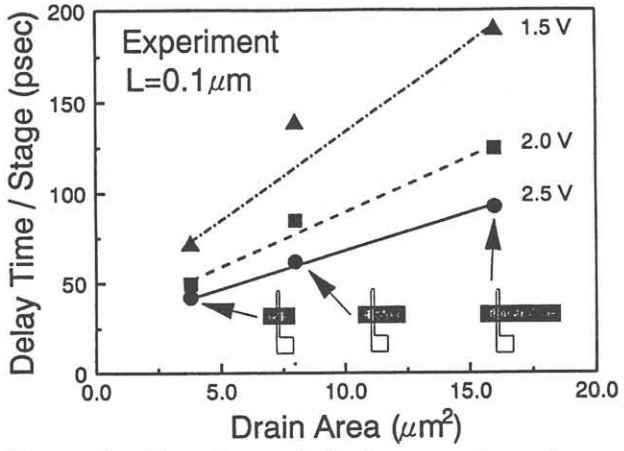


Figure 1: Experimental drain area dependence of propagation delay time in 0.1 $\mu$m gate length CMOS ring oscillator at $V_{DD}$=1.5 V,2.0 V and 2.5 V, respectively.

1.4 $V \leq V_{DD} \leq 2.5\ V$. In this power-delay relationship, an increase in the drain area degrades only $\tau_{pd}$ with little change in power dissipation under a fixed $V_{DD}$. This means that the junction capacitance itself contributes to the degradation of $\tau_{pd}$ but it does not influence power dissipation. These facts bring a total increase in the power-delay product, as shown in Fig 2. The drain junction capacitance effect on the power-delay product also estimated by using the circuit simulator SPICE. If the drain junction capacitance is reduced to 1/10 of the present value, the power-delay product will be reduced to the broken line in Fig.2. Moreover, various parasitic effects on

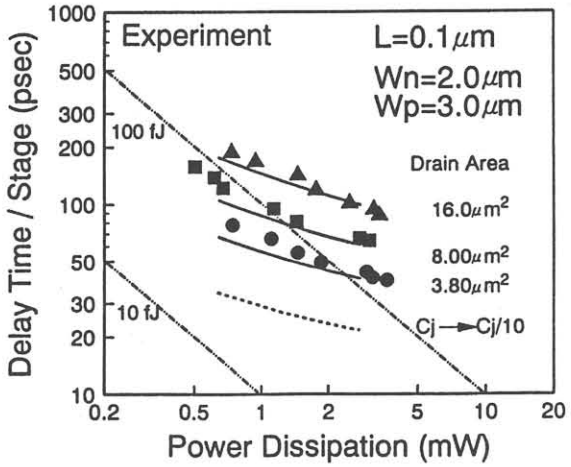


Figure 2: Relationship between propagation delay time and power dissipation of 0.1 $\mu$m gate length CMOS devices for three drain areas. Solid lines show the results of SPICE simulation. Broken line shows the simulated result for junction capacitance reduction to 1/10 of present $C_j$ value.

$\tau_{pd}$ were investigated by circuit simulation. Figure 3 shows the various components in $\tau_{pd}$ at $V_{DD} = 2.5\ V$ and 1.5 $V$, which were calculated with SPICE, in which the device model parameters were extracted from the measured DC characteristics of the 0.1 $\mu$m CMOS devices, junction capacitance, and gate resistance. In the 0.1 $\mu$m gate length CMOS devices,

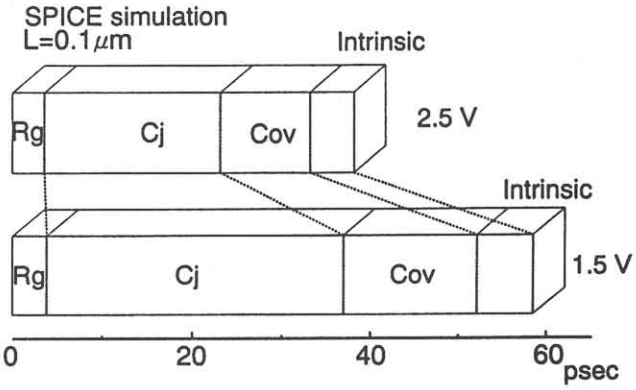


Figure 3: Schematic representation of various components in propagation delay time of 0.10 $\mu$m gate length CMOS devices at 2.5 V and 1.5 V.

junction capacitance reduction is necessary both for higher switching speed and lower power-delay product, especially for low voltage operation. We can realize $C_j$ reduction by using a low impurity concentration substrate beneath the source/drain area or by miniaturizing of the source/drain area. However, other parasitic effects such as contact resistance effect will emerge by miniaturizing of the device configuration. Such an effect will be discussed in the following section.

## 3 Contact Resistance Effect on Scaled 0.1 $\mu$m CMOS Devices

The dimensions of the 0.1 $\mu$m gate length CMOS devices described above were not fully scaled down to the 0.1 $\mu$m level, therefore they receive little influence from the contact resistance. Although the shrinkage of the drain area can drastically improve $\tau_{pd}$, it will degrade $\tau_{pd}$ in scaled 0.10 $\mu$m CMOS devices due to an increase in the contact resistance. Such contact resistance effect on $\tau_{pd}$ was investigated by using SPICE. In the simulation, the contact resistance $R_c$ was assumed to be a specific contact resistance $\rho_c$ divided by the contact size $K$ ( i.e. $R_c = \rho_c(\Omega\text{cm}^2)/K^2(\text{cm}^2)$). The current crowding effect on $R_c$ was neglected for simplicity. It was also assumed that both NMOSFETs and PMOSFETs had the same contact size $K$ and the same specific contact resistance $\rho_c$. It was further assumed that the contact resistance of the gate electrode was small and was able to be neglected in the simulation. In the limit of zero contact resistance, it has been found that $\tau_{pd}$

is less than 20 psec and the power-delay product is less than 10 fJ in fully scaled 0.1 $\mu$m CMOS devices. In this case, the delay time decreases with junction area reduction, which is shown by the solid line in Fig.4. Next, the contact resistance effect on $\tau_{pd}$ was considered. It is clearly shown in Fig.4 that though $\tau_{pd}$ is reduced by the reduction of $C_j$, a minimum $\tau_{pd}$ in fact exists as a function of $\rho_c$ in a larger device configuration than the fully scaled 0.1 $\mu$m device under a given $V_{DD}$.

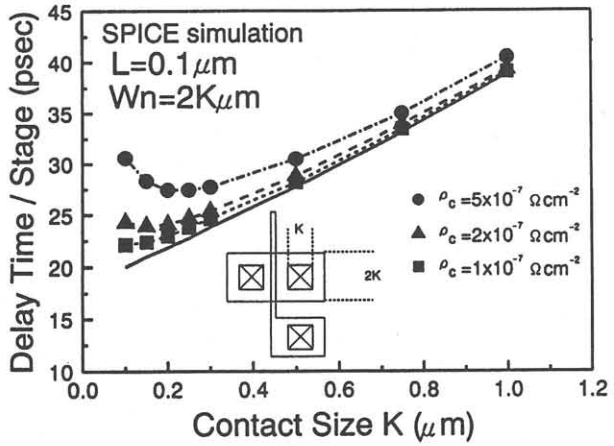


Figure 4: Influence of source/drain contact resistance on propagation delay time in 0.1 $\mu$m gate length CMOS ring oscillator with changing contact size and junction area. Individual gate contact resistances were neglected in these simulations.

The minimum device configuration depends both on $\rho_c$ and the junction capacitance per unit area($C_{j0}$). If we use a low impurity concentration substrate to reduce $C_{j0}$, the fastest switching device configuration of a 0.1 $\mu$m CMOS becomes much larger than the minimum configuration shown in Fig.4. Therefore, the condition for the fully scaled 0.1 $\mu$m CMOS device to have a faster switching speed than larger size 0.1 $\mu$m CMOS devices was investigated. In other words, the condition that the miniaturizing of a device size maintains the advantage of a higher switching performance in this 0.1 $\mu$m era was searched. Figure 5 shows the critical condition that $\rho_c$ and $C_{j0}$ should be decreased so as to achieve fastest $\tau_{pd}$ in fully scaled down 0.1 $\mu$m devices. For example, if $\tau_{pd}$ must be less than 20 psec in the fully scaled 0.1 $\mu$m CMOS devices, $C_{j0}$ and $\rho_c$ are required to be less than about 1.0 fF/$\mu$m$^2$ and $1.0\times10^{-7}\Omega$cm$^2$.

This fact means that the specific contact resistance currently used both for NMOSFETs and PMOSFETs is not satisfactory in fully scaled 0.1 $\mu$m CMOS devices, and further improvement is required. Otherwise, scaling the device sizes down will in practice degrade speed performance.

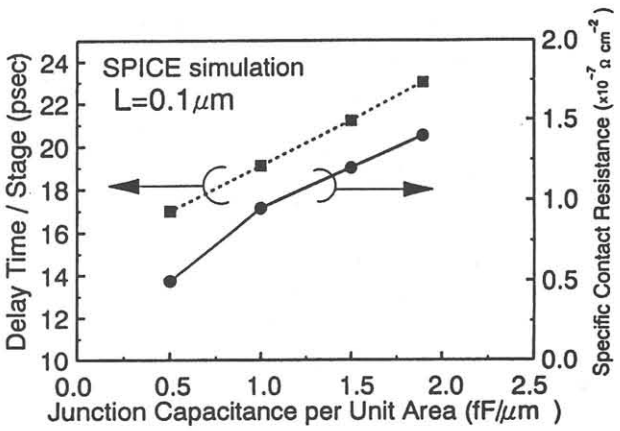


Figure 5: Relationship between propagation delay time, specific contact resistance, and junction capacitance per unit area for achieving the fastest speed in a fully scaled down 0.1 $\mu$m CMOS device. The contact size K was set to 0.10 $\mu$m, and the source/drain area was set to 0.04 $\mu$m$^2$.

## 4 Conclusion

Both the contact resistance $\rho_c$ and the junction capacitance $C_{j0}$ for the source/drain region have significant effects on switching performance in this fully scaled down 0.1 $\mu$m device era. For higher switching performance, they must be taken into consideration. This study demonstrates that $\rho_c$ should be less than $\sim 1\times10^{-7}\Omega$cm$^2$, otherwise the scaling down advantage will be deteriorated in this 0.1 $\mu$m era.

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