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# Universal Behavior of Hot-Carrier Degradation in LDD NMOSFET's

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## Abstract

This paper experimentally demonstrates that hot carrier degradation curves of LDD NMOSFET's for different stress conditions fall on a universal curve which makes accurate lifetime prediction possible using conventional $\log(\tau I_d)$ vs. $\log(I_{sub}/I_d)$ method even if the degradation vs. stress time curves show a saturation behavior. A modified mobility model with a lower limit parameter for mobility degradation has been developed, which successfully describes the saturation behavior of device degradation.

## 1. Introduction

Hot-carrier induced MOSFET degradation leading to long-term instabilities is one of the major limitations on the scaling of device size [1,2]. To estimate the long-term reliability of NMOS, several lifetime prediction methods based on the lucky electron model and an empirical power-law dependence of the degradation on stress time have been widely used [3,4]. However, recent reports suggest that, due to barrier ($\Phi_{it}$) enhancement mechanism, the hot-carrier degradation saturates after certain threshold value instead of following a simple time-power-law so that the lifetime prediction method using $\log(\tau I_d)$ vs. $\log(I_{sub}/I_d)$ graph is no longer valid [5,6].

In this paper, physical mechanism for the saturation behavior of degradation in LDD NMOS is investigated with the help of experiments and simulations. Also, a simplified lifetime prediction method using the universal behavior of hot carrier degradation curve is developed.

## 2. Experimental

LDD NMOSFETs with $L_{eff}$ = 0.35μm, $W_{eff}$ = 50μm, and $T_{ox}$ = 100Å were fabricated using the conventional twin-well CMOS process. Phosphorus n$^-$ implants were performed at 40 keV. Then, 100nm oxide spacer was formed before high dose As implant with 0.2μm junction depth to produce fully overlapped LDD structure. The MOSFETs were hot-carrier stressed at the maximum $I_{sub}$ condition. After the hot-carrier stress, degradation of $V_{th}$, $G_m$, $I_{dl}$ (linear current) and $I_{dsat}$ (saturation current) was monitored in reverse mode (source and drain were exchanged). All of these parameters were measured at room temperature.

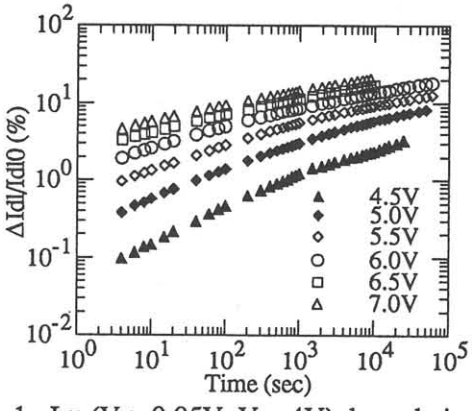


Fig. 1. $I_{dl}$ ($V_d$=0.05V, $V_g$=4V) degradation vs. stress time for LDD NMOS stressed at voltages between $V_d$=4.5V and $V_d$=7.0V ($V_g$= maximum $I_{sub}$ condition).

## 3. Results and Discussion

Fig. 1 shows $I_{dl}$ degradation curves as a function of stress time. $\Delta V_{th}$ was negligible for these stress conditions. It can be seen that the degradation curves show a tendency to saturate at higher drain voltages and longer times. If the simple time-power-law based curve fitting is applied to these experimental data for lifetime prediction, the resulting $\log(\tau I_d)$ vs. $\log(I_{sub}/I_d)$ graph (Fig. 2) does not show a good linearity. Further, the gradient of lifetime curve ($\Phi_{it}/\Phi_i$) increases as the critical degradation amount for device failure criterion decreases. Therefore, if the lifetime of device at operation voltage ($V_d$ = 3.3V) is extrapolated from Fig. 2, the lifetime for 1% degradation will turn out to be longer than the lifetime for 10% degradation, which will be an incorrect result.

To overcome this difficulty, we suggest the following method which uses the universal behavior of degradation curves. Fig. 3(a) is produced by shifting

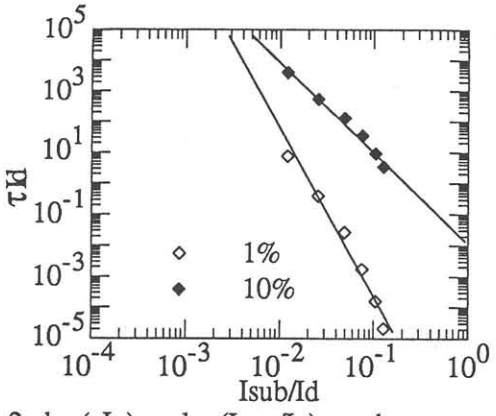


Fig. 2. $\log(\tau I_d)$ vs. $\log(I_{sub}/I_d)$ graph generated from Fig. 1 using simple time-power-law based curve fitting (1% and 10% $I_{dl}$ degradation).

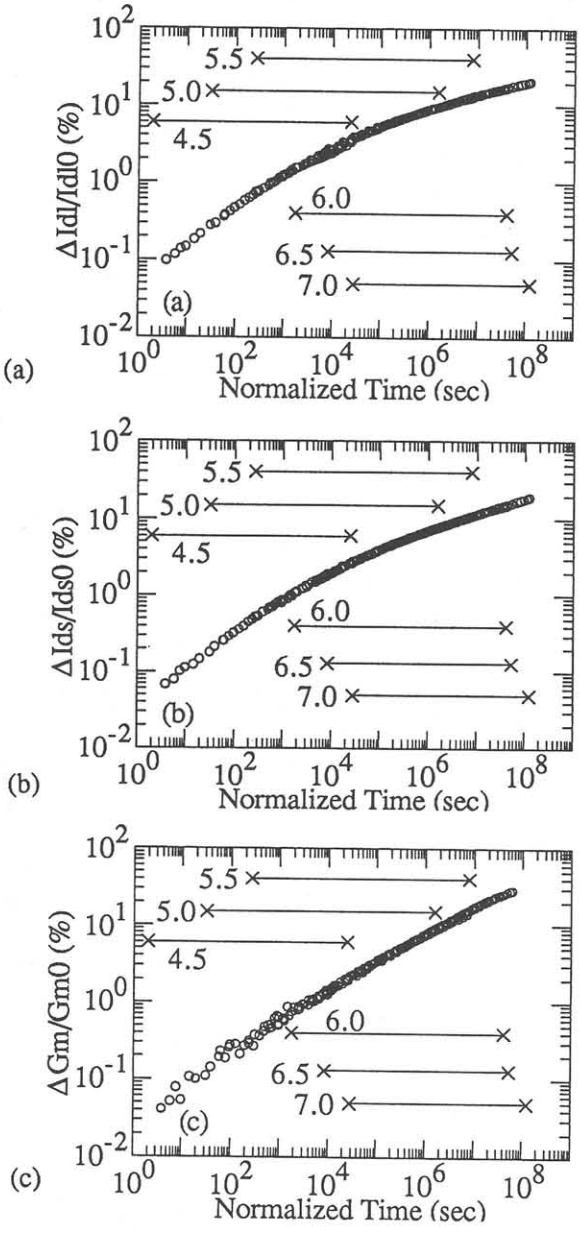


Fig. 3. Degradation vs. normalized stress time for the device of Fig. 1. Same time shift factor was used for three graphs. The range in time of each stress is shown.

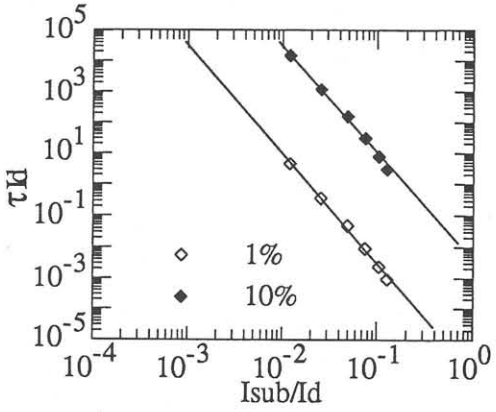


Fig. 4. $\log(\tau I_d)$ vs. $\log(I_{sub}/I_d)$ graph generated from Fig. 1 using the proposed method (1% and 10% $I_{dl}$ degradation).

each degradation curve (Fig. 1) in x axis (time) by a series of constants such that identical values of $\Delta I_{dl}/I_{dlo}$ from each curves coincide. Same series of constants were applied for $G_m$ and $I_{dsat}$ degradation curves and they resulted in a similar single smooth line (Fig. 3(b),(c)). The alignment of these overlapped curves to a single curve supports the argument that the behavior at low and high drain voltages is all part of an overall "universal" curve. This universal behavior of degradation implies that the gradient of degradation curves depends only on the amount of existing damages such as the interface state ($N_{it}$). Similar result for PMOS was also reported [7]. In that paper, an empirical lifetime prediction method based on $V_d$ was suggested. However, the universal behavior of LDD NMOS implies that $E_m$ or $\Phi_{it}$ does not change during the stress [8]. Therefore, even if the degradation curves show a saturation behavior, the use of $\log(\tau I_d)$ vs. $\log(I_{sub}/I_d)$ graph is still valid to predict the lifetime at the operation voltage as long as the lifetime at each accelerated drain stress voltage is accurately determined. Fortunately, this accurate determination is guaranteed by the universal behavior of degradation curves. If we experimentally measure the lifetime at one of the accelerated drain stress voltage, the lifetime at other drain voltages can be accurately determined from the amount of time shift required to lay one degradation curve on the top of

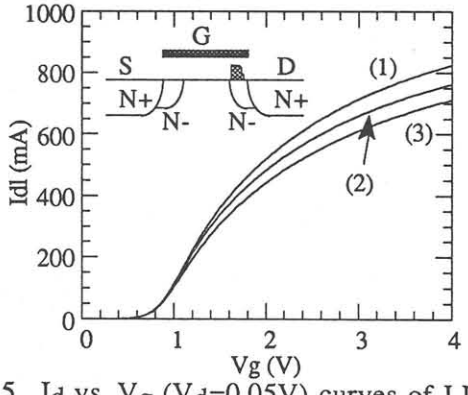


Fig. 5. $I_d$ vs. $V_g$ ($V_d$=0.05V) curves of LDD NMOS before and after a hot carrier stress of $V_d$=6V and $V_g$=2.3V (measurement was done in reverse mode). (1) the initial curve, (2) after $2x10^3$ sec, (3) after $6x10^4$ sec.

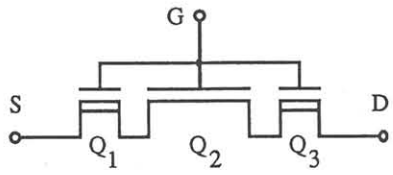


Fig. 6. Schematic diagram of equivalent circuit for LDD NMOS. Due to the localization of $N_{it}$ generation in LDD $n^-$ region, LDD NMOS can be separated into one enhancement transistor ($Q_2$) for channel region and two depletion transistors ($Q_1$, $Q_3$) for source/drain region.

another curves. Fig. 4 is produced by applying this method to the data shown in Fig. 1. It shows much better linearity in comparison to Fig. 2 and two curves for two different degradation criteria (1% and 10%) are parallel to each other.

The degradation of linear $I_d$-$V_g$ characteristics after hot carrier stress is shown in Fig. 5. In comparison to the well-known behavior of stressed single drain structure (simultaneous degradation of $V_{th}$ and $I_{dl}$) [9,10], LDD structure shows negligible $V_{th}$ shift, even if $I_{dl}$ at $V_g$=4V shows more than 10% degradation. This difference can be explained by the location of generated interface state. In LDD structure, $N_{it}$ is generated only on the $n^-$ region (inset of Fig. 5) during the initial stage of stress. Therefore, only $I_{dl}$ at high $V_g$ condition starts to degrade due to the increase of series resistance in $n^-$ region. After extensive stress, $N_{it}$ will spread out to the channel region, and so, $V_{th}$ will start to shift. Due to this unique behavior (localization of $N_{it}$ generation in $n^-$ region) of LDD structure after stress, it is possible to study the degradation mechanism of LDD structure using the equivalent circuit shown in Fig. 6. Various SPICE simulations were done to match the simulated $I_d$-$V_g$ curves to the experimental data measured after hot-carrier stress by applying a modified mobility degradation model to the depletion transistor $Q_1$ representing the source $n^-$ region (degradation measurement was done in reverse mode).

$$\mu/\mu_O = \delta + (1 - \delta) / (1 + \gamma t^n)$$

where, $\delta$ = lower limit of mobility degradation

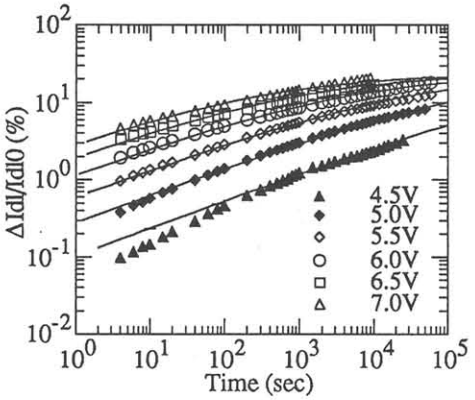


Fig. 7. Experimental (symbol) and model (line) results of $I_{dl}$ ($V_d$=0.05V, $V_g$=4V) degradation at stress voltages between $V_d$=4.5V and $V_d$=7.0V. The fitting parameter values are $\delta$ = 0.18, n = 0.358, and $\gamma$ = 0.019 - 0.59.

In comparison to the channel inversion layer, the carrier distribution in LDD $n^-$ accumulation layer is deeper away from the $Si/SiO_2$ interface, so it is expected that the mobility degradation due to $N_{it}$ may have a lower limit. Therefore, the model described above was derived from the well-known mobility degradation model ( $\mu/\mu_O = (1+\alpha N_{it})^{-1} = (1+\gamma t^n)^{-1}$ ) [11] by adding a lower limit parameter ($\delta$) for mobility degradation. As can be seen in Fig. 7, the agreement between the simulation and the experimental data is very good and the saturation behavior at high $V_d$ is also well reproduced by this model.

## 4. Conclusion

It is experimentally demonstrated that the hot carrier degradation curves of LDD NMOS or different stress condition fall on a universal curve and the $\log(\tau I_d)$ vs. $\log(I_{sub}/I_d)$ graph can be used for lifetime extraction even if the degradation vs. stress time curves show a saturation behavior. Analysis of $I_d$-$V_g$ characteristics after hot-carrier stress shows that only the $I_d$ at high $V_g$ condition start to decrease with negligible $V_{th}$ shift, which is due to the localization of $N_{it}$ generation in $n^-$ region. It is also shown that a modified mobility degradation model successfully reproduces the saturation behavior of degradation curves.


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