Reliability of nm-Oxide Formed on Si Wafers Containing Crystal Defects

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MOS capacitors fabricated on Si wafers having intentionally formed crystal defects are evaluated. The defects introduced are oxidation induced stacking faults (OSF) and micro defects (MD) caused by oxide precipitate. Using time dependent dielectric breakdown (TDDB) measurement results, oxide reliability was quantitatively analyzed, showing that OSF causes time-zero breakdown, MDs can cause weakspots in oxide (weakspot:MD ratio = 1:100), and reliability of thin oxide, less than 10 nm, remains excellent even in the presence of crystal defects.

INTRODUCTION:

In submicron LSIs, gate oxide reliability has become more and more serious with increasing integration scale, for three reasons. The electric field within the oxide tends to increase as the film thickness is reduced, the oxide is formed on a sharp isolation edge due to the advanced isolation technique¹⁾, and the To obtain a guideline to chip area is larger. improve oxide reliability, it is important to characterize the oxide reliability quantitively. On the other hand, crystal defects induced in LSI processes have been thought to be one of main origins of the weakspot in gate oxide²). In this study, MOS capacitors fabricated on Si wafers having intentionally formed crystal defects were evaluated to quantitatively clarify the role of crystal defects effect-on oxide reliability. The defects introduced are oxidation induced stacking faults (OSF) and micro defects (MD) caused by oxide precipitate³⁾⁴⁾. Using time dependent dielectric breakdown (TDDB) measurement results, oxide reliability was quantitatively evaluated by comparing defect densities with weakspot thicknesses and weakspot densities.

SAMPLE PREPARATION:

Crystal defects were formed in Si wafers during 1-µm-thick pyrogenic oxidation at 1100°C (Fig. 1). Distinct MD swirl patterns (Fig. 2a) were observed in about 50% of the oxidized wafers. These wafers will be referred to as MD wafers hereafter. After removing the thick oxide, some wafers were re-oxidized under the same conditions. OSFs, as shown in Fig. 2b, are formed in all the re-oxidized MD wafers. These wafers will be referred to as OSF wafers. MOS capacitors were fabricated using these two types of wafers as starting materials. A mesa type capacitor was fabricated to avoid the influence of crystal defects induced by field oxidation.

ANALYSIS METHOD:

We assume that the gate oxide breakdown occurs at the weakspot in the oxide. The weakspot is the point where the oxide thickness is locally reduced and hence electric field is enhanced, as schematically shown in Fig. 3^{5}). The normalized weakspot thickness X = $d_w / d_{ox} (d_w :$ oxide thickness at the weakspot, d_{ox} : intrinsic oxide thickness) and the weakspot density for each X, D(X), are extracted from TDDB data. X and D(X) can be written in the form of general expressions when the distribution of the weakspots is assumed to be Poissonian⁶)

$1/X = Ti^{-1}(t_{bd}) / E_s$

where Es is the stress field, t_{bd} is breakdown time and Ti is the intrinsic breakdown time CZ p-type Si wafer (100), 10Ω.cm



Fig. 1 Sample Preparation Process

which is a function of the field.

 $D(X) = \ln \left(1 - F_{tbd}\right) / S,$

where F_{tbd} is the failure rate at time t_{bd} , and S is the capacitor area.

The oxide reliability can be quantitatively evaluated by extracting X and D(X).

RESULTS:

Figure 4 shows the distribution of breakdown voltage (gate voltage which causes leakage current of 10⁻⁶A / cm²). For 10-nmthick oxide, both MD and OSF wafers lower the breakdown voltage compared with the reference wafer. In particular, OSF wafer leads to a large number chip failures. This means that OSF induces time-zero breakdown defects in the oxide. The lowering of breakdown voltage in 6-nm-thick oxide is much smaller.

X is found to depend on MD densities obtained from Secco etching⁷)(Fig. 5). When the MD density exceeds 10^6 /cm², X decreases abruptly. This means that MDs degrade oxide reliability only when over 100 MDs are observed by Secco etching in one capacitor (capacitor area: 10^{-4} cm²).

Figure 6 shows the relationship between X and D(X) extracted from capacitors with various areas. The data from all the capacitors on the reference wafer fit on an identical line. Hence, the assumption that the weakspot distribution is Poissonian is reasonable. In the reference wafer, X begins to decrease at D(X)as low as $10/\text{cm}^2$, compared to $10^3/\text{cm}^2$ MD in the reference wafer. These values



Fig. 2 Schematic images of crystal defects distribution







Gate voltage Vg at the leakage current density of $Jg = 10^{-6}$ A / cm²

Fig.4 Distributions of breakdown voltage

(weakspots:MD ratio=1:100) are in good agreement with the result in Fig. 5, and indicate that the main origin of weakspots in LSI processes are MDs.

On the other hand, for MD and OSF wafers, the weakspots do not follow a Poisson distribution. This is because the crystal defects are distributed over the wafer as shown in Fig. 2. This produces the reliability (equivalent to breakdown time) distribution on the wafer shown in Fig. 7. It is interesting that the weakspot thickness in the OSF wafers is larger than that in MD wafers. This result indicates that the MD densities in OSF wafers are smaller than those in MD wafers, which is also confirmed by Secco etching. Like Fig. 4, the increase in weakspot densities is less for 6-nm oxide than for 10-nm oxide. So the reliability of thin oxide less than 10-nm still remains excellent even when crystal defects exist.



Fig.5 Normalized weakspot thickness, X vs. MD densities



Fig. 6 Weakspot densities vs. weakspot thickness on the MD and OSF wafers

CONCLUSIONS:

A comparison of the densities of both crystal defects and weakspots in oxide, showed that OSF causes time-zero breakdown defects in oxide, MDs probably cause the weakspots in oxide (weakspot:MD ratio= 1:100), which determine the oxide reliability in standard LSI processes, and the reliability of thin oxide less than 10-nm remains excellent even in the presence of crystal defects.

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Fig. 7 Distribution of breakdown times in TDDB measurement