Extended Abstracts of the 1993 International Conference on Solid State Devices and Materials, Makuhari, 1993, pp. 835-837

Temperature Effects of the Inversion Layer Electron and Hole Mobility of MOSFETs from 85K to 500K

J.S. Duster, Z.H. Liu, P.K. Ko, and C. Hu
Dept. of EECS, University of California
University of California, Berkeley, CA 95720

Abstract - A comprehensive study of the low field inversion layer mobility from 85K to 500K has been undertaken. NMOS and PMOS devices over a wide range of process and bias conditions were used to isolate different scattering mechanisms. At moderate doping levels ($<10^{17}$ cm^{-3}) and electric fields ($<3x10^5$ V/cm), the mobility is limited by phonon and interface coulomb scattering α $T^{-2/3}$ below 150K, and by phonon and surface roughness scattering α $T^{-3/2}$ at higher temps and fields. Highly doped devices, limited by bulk coulomb and surface roughness scattering, show marginal temperature dependence below 150K. The mobility limited by coulomb scattering displays a T_{ox} dependence below 200K. The impact of charge injection into the oxide on mobility was also investigated.

1. INTRODUCTION

The inversion layer mobility is one of the most important parameters of an MOS device[1][2] This work presents a comprehensive study of the temperature characteristics of the low longitudinal field effective mobility of electrons and holes in the inversion layers of MOSFETs over an extended temperature range from 85K to 500K in 50K increments for a very broad set of devices.

The device parameters cover oxide thickness values ranging from 50 to 450Å, for each of 4 doping levels: from $2.4x10^{16}$ to $1.7x10^{18}$ cm^{-3}. The mobility is measured at effective vertical fields from 10^5 to $1.5x10^6$ V/cm for both n-channel and p-channel transistors making this data set truly applicable for current and future deep submicron modeling. By encompassing such a wide range of parameters, the individual components of the scattering mechanisms which determine the mobility can be clearly identified.

An oxide thickness dependence of the low field mobility at temperatures below 200K has been observed, and the mobility of very highly doped n-channel transistors is independent of temperature below 150K. An investigation of the interface characteristics has been undertaken to reveal insights into this phenomena. A direct correlation between the stress induced interface state generation and mobility degradation has been verified by constant current injection experiments performed on devices at elevated, ambient, and reduced temperatures.

2. MOBILITY MEASUREMENT & DISCUSSION

The effective mobility (V_{DS} = 50 mV) was extracted using the split CV technique [3] to correctly extract the inversion charge. The electron and hole mobility for lightly doped cases (Figs. 1 & 2) clearly show decreases in the peak mobility for the thinner oxide devices for electrons, and to a smaller extent for holes, at temperatures lower than 200K. At LN temp, the peak mobility for a lightly doped NMOS devices is degraded by nearly 25% as T_{ox} is reduced from a 450 to 50Å. As the doping level is increased the magnitude of the reduction is decreased.

The substrate doping level, temperature, and electric field dictate which of the dominant scattering mechanisms will be prevalent. For lightly and moderately doped devices ($N_B < 10^{17}cm^{-3}$) biased at moderate vertical electric fields (Fig. 3 & 4) phonon scattering is the dominant mechanism - $T^{-3/2}E^{-1/3}$ for temperatures above 150K. As the temperature is reduced, surface roughness scattering begins to dominate at ever lower electric fields and the mobility falls of more rapidly - E^{-2} for electrons (and E^{-1} for holes). However, for very highly doped devices, surface roughness scattering is predominant even at higher temperatures and the mobility falls off as E^{-2} (and E^{-1}) although the temperature dependence of the phonon scattering $T^{-3/2}$ remains.

As the temperature is reduced, the mobility of lightly doped transistors biased 300 KV/cm above the peak of the low temperature mobility increases with decreasing temperature (Fig. 5). However, for highly doped NMOS

devices only marginal increases in the mobility are observed as the temperature is reduced below 200K. The temperature trends for p-channel devices are similar to those for n-channel, however the mobility at high doping levels still increases below 200K in contrast to the NMOS case.

For devices operating at low relative transverse electric fields, where coulomb scattering is predominant, the scattering of the inversion layer carriers by the bulk ionized impurities increases with the doping level. The mobility of n-channel devices doped > $6x10^{17}cm^{-3}$ is independent of temperature below 200K because the bulk dopants are no longer effectively screened (phonon scattering $\propto T^{-3/2}$ and bulk coulomb scattering $\propto T^{3/2}$)[4]. The limit from surface roughness scattering displays no temperature dependence. For lightly doped transistors the density of bulk dopant ions is small enough to be effective screened by the inversion layer carriers. For devices doped < $10^{17}cm^{-3}$ the spatial density of scattering sites at the interface approaches that of the dopant ions (for inversion layer thickness ~ 50 Å), and coulomb scattering near the interface cannot be neglected for such devices.

3. F-N STRESSED DEGRADATION

Charge pumping and C-V measurements on fresh samples revealed D_{it} near $5x10^9$ $cm^{-2}eV^{-1}$ which varied very little with oxide thickness. In addition to the screening of ionized impurities in the substrate, the inversion layer carriers must also screen scattering sites at the Si/SiO_2 interface. This scattering mechanism $\propto T^{2/3}$, which is more prevalent for lightly doped devices, shows different characteristics than the bulk coulomb scattering and must be modeled separately.

To study this, interface states were generated by constant current injections (0.2 $mAcm^{-2}$) performed at 300K and 85K. The room temperature stresses produced moderate reductions in the peak mobility at 300K, and increasingly larger degradation as the measurement temperature was reduced to 85K (about 70% greater the the reduction at 300K) as the masking effect of phonon scattering is attenuated. However, injecting the same charge at low temperature produced very little change in the peak mobility (Figs 6-8). To achieve the same degradation as a room temperature stress, an LN temp stress takes almost a order of magnitude longer for 90Å devices, but does generate the same level of interface states. The electron mobility does not display appreciable degradation until the generated trap densities exceed $2x10^{10}$ $cm^{-2}eV^{-1}$.

As the substrate doping level is reduced (Fig. 7), less interface states (and shorter stress times) are necessary to maintain a similar level of degradation. In addition, for thicker oxides (Fig. 8), shorter 300K stressing periods yield equal percentage degradation, but the ratio of LN stress time to 300K stress time for similar reductions in mobility increases. Identical experiments were performed on p-channel devices whose mobility's were reduced by smaller interface trap generation than the corresponding nMOSFETs.

4. REFERENCES

[1] S.C. Sun and J.D. Plummer, IEEE Trans. Electron Devices, 27(1980) 1497.

[2] A. Hairapetian, et al., IEEE Trans. Electron Devices, 36(1989) 1448.

[3] M.S. Liang, et. al., IEEE Trans. Electron Devices, 33(1986) 409.

[4] K. Seeger, Semiconductor Physics, New York: Springer-Verlag, (1989) ch. 6.

5. FIGURES

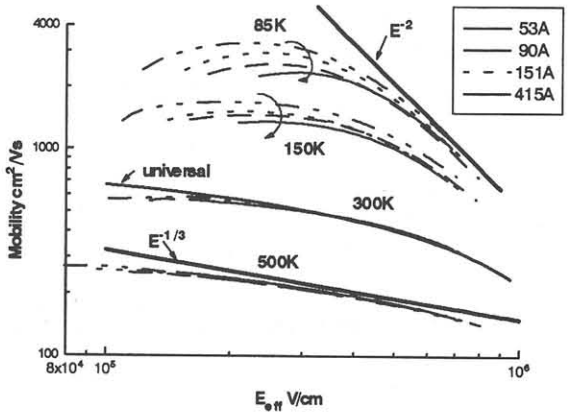

Fig. 1 The effective electron mobility versus effective field measured from 85K to 500K for nMOSFETs. N_B=2.4x10^{16}cm^{-3}, W/L = 100 µm/28 µm, and T_{ox} ranges from 53Å to 415Å. Peak mobility shows oxide thickness dependence.

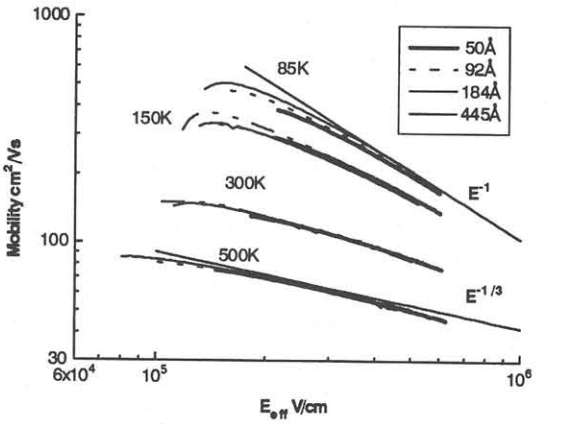

Fig. 2 The effective hole mobility versus effective field measured from 85K to 500K for pMOSFETs. The device parameters are N_B=3.5x10^{16} cm^{-3}, W/L = 100 µm/28 µm, and T_{ox} ranges from 50Å to 445Å.

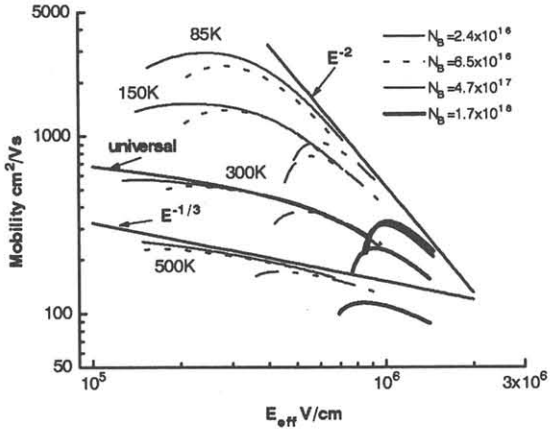

Fig. 3 Effective mobility of electrons versus effective electric field for devices over the temperature range 85K to 500K with N_B varying from $2.4x10^{16}$ cm^{-3} to $1.7x10^{18}cm^{-3}$. All of the devices had $T_{ox} \approx 145Å$ and W/L = 100 μm/ 28 μm .

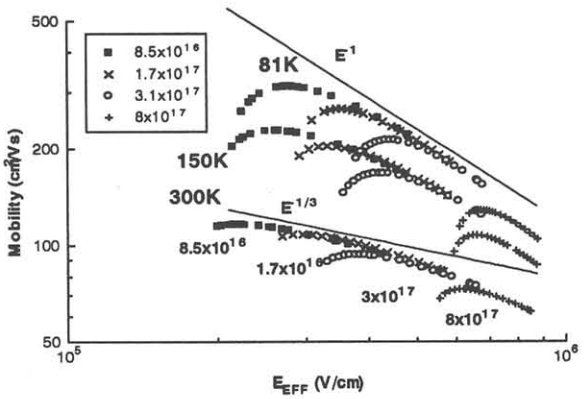

Fig. 4 Hole mobility versus effective electric field for devices over the temperature range 81K to 300K. $N_B = 8.5x10^{16}$ cm^{-3} to $8x10^{17}cm^{-3}$. $T_{ox} \approx 110Å$ and W/L = 70 μm/ 20 μm .

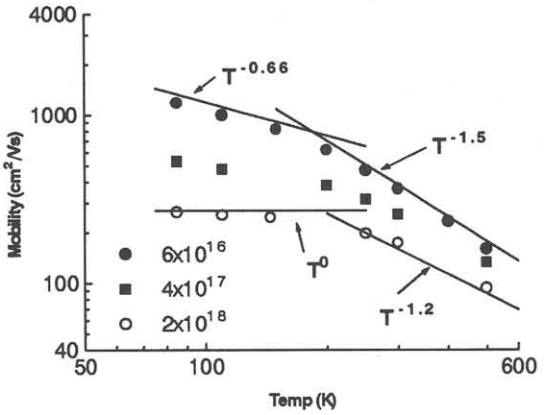

Fig. 5 Electron mobility measured at different temperatures from moderate to very highly doped substrates emphasizing the temperature dependencies of phonon, coulomb, and surface roughness scattering. Device parameters are $N_B = 6x10^{16}cm^{-3}$ to $1.7x10^{18}cm^{-3}$, T_{ox}=145Å, and W/L=100 μm/ 28μm.

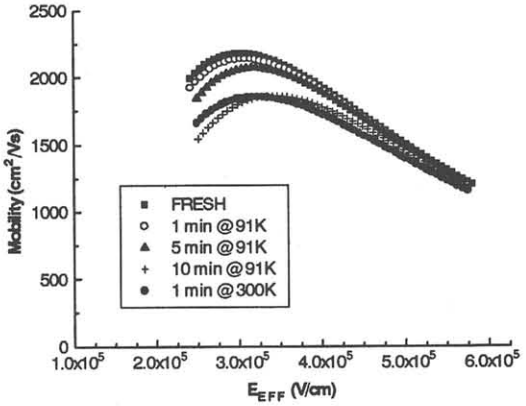

Fig. 6 Electron mobility measured at 91K for Substrate Hot Electron stress at 91K and 300K. The device parameters are $N_B = 6x10^{16}cm^{-3}$, T_{ox}=94Å, and W/L=100 μm/ 10μm.

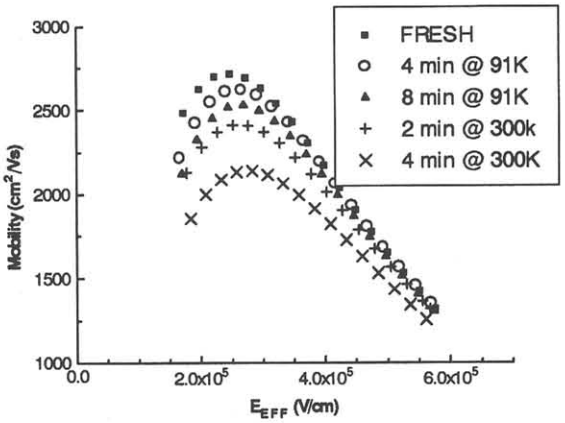

Fig. 7 Electron mobility measured at 91K for Substrate Hot Electron stress at 91K and 300K. The device parameters are $N_B = 2.4x10^{16}cm^{-3}$, T_{ox}=90Å, and W/L=100 μm/ 10μm.

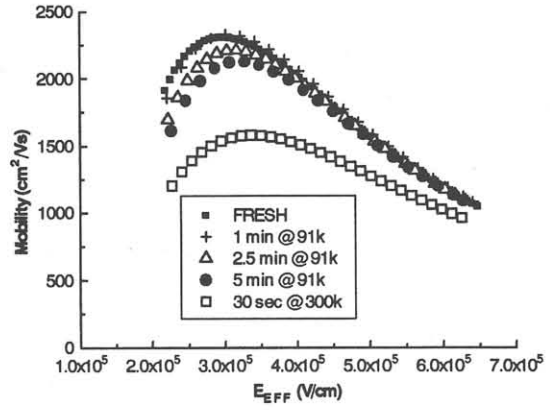

Fig. 8 Electron mobility measured at 91K for Substrate Hot Electron stress at 91K and 300K. The device parameters are $N_B = 6x10^{16}cm^{-3}$, T_{ox}=145Å, and W/L=100 μm/ 10μm.