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Degradation Phenomenon under Low Drain Voltage Stress in pMOSFETs

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Hot carrier degradation in pMOSFETs under low drain voltage stress has been investigated. The degradation is especially enhanced in pMOSFETs with thin gate oxide(~ 10nm) under the repeated conditions of high gate and low drain voltage stress(HG stress) where drain current is not flowing and avalanche hot carrier stress(AHC stress). A large number of new trap centers are generated by avalanche hot electron injection into the gate oxide, and then holes are injected into the new trap centers in the gate oxide above the drain even during short high gate and low drain voltage stress time. It should be noted that CMOS inverter operations in LSI circuits contain HG stress conditions. Much attention has to be paid to this result for reliable device design.

I. Introduction

As device dimensions are scaled down, hot-carrier-induced degradation has become the most serious constraint in realizing high reliability for half micron MOSFETs. Recently, enhanced degradation of nMOSFETs under avalanche hot carrier [AHC] injection and subsequent channel hot electron [CHE] injection[1] has been reported. However, only a few studies have referred to the degradation of pMOSFETs under AHC stress and subsequent HG(high gate and low drain voltage) stress.

This paper reports a new enhanced degradation phenomenon under HG stress where drain current is not flowing in LDD pMOSFETs with thin gate oxide(~10nm). This enhanced degradation of pMOSFETs occurs even during short HG stress time. It should be noted that CMOS inverter operations in LSI circuits contain HG stress conditions. Much attention has to be paid to this result for reliable device design.

II. Experimental and Results

LDD pMOSFETs were fabricated by a conventional polysilicon-gate CMOS process. The test device had a gate length of 0.6 μ m, gate width of 12 μ m, gate oxide thickness of 10nm, and sidewall thickness of 0.15 μ m. AHC stress and HG stress were repeatedly applied to the test devices. For the AHC stress conditions, the gate voltage(Vg) is -1.5V, the drain voltage(Vd) is -6V and the source voltage(Vs) is fixed at 0V. For the HG stress conditions, Vg is -6V, both Vd and Vs are fixed at 0V. The waveforms under repetition of AHC stress and HG stress (repeated stress) are shown in the insert in Fig.1. The degradation under repeated stress was compared with that under only AHC stress. AHC stress time dependence of threshold voltage shifts(Δ Vt) as a function of HG stress time is shown in Fig.1. HG stress time are varied from 256 seconds to 32000 seconds.

Δ Vt under repeated stress is more enhanced than that under only AHC stress. For example, obvious difference of Δ Vt between repeated stress and only AHC stress is observed after the stress of 10^5 seconds in Fig.1.

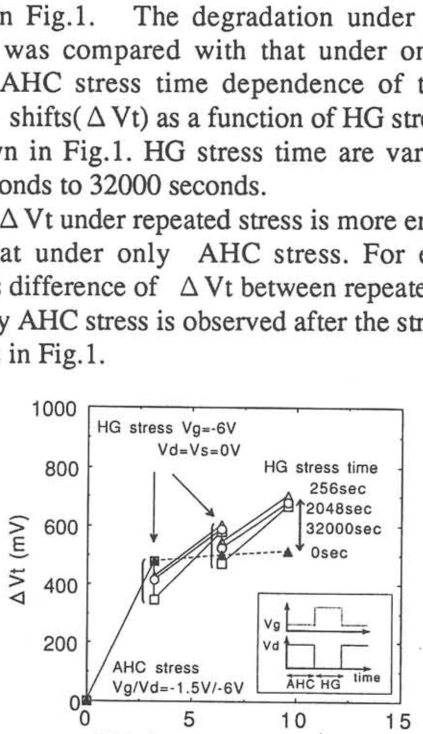

Fig.1. ΔVt as a function of HG stress time
(HG stress is high gate and low drain voltage stress)
: under repetition of AHC stress and HG stress
vs only AHC stress

Vt shifts of 700mV under repeated stress and Vt shifts of 500mV under only AHC stress are observed, respectively. Slight difference in Δ Vt between long and short HG stress time is observed. Moreover, the degradation under repetition of AHC stress and channel hot hole[CHH] stress was investigated. The degradation under CHH stress was compared with that under HG stress in Fig.2. For the CHH stress conditions, both Vg and Vd are -6V, Vs is fixed at 0V. As for enhanced degradation by repetition of AHC stress and CHE stress in nMOSFETs, T.Tsuchiya et al. have already reported[1]. Vt shifts by repetition of AHC stress and HG stress is more enhanced than that by repetition of AHC stress and CHH stress.

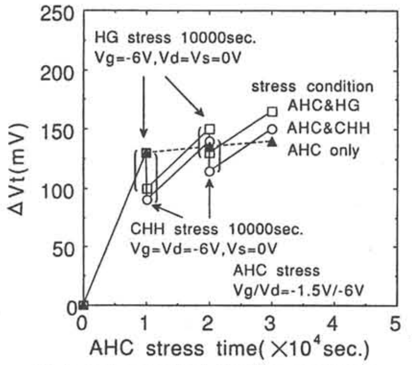

Fig.2. Δ Vt dependent of stress conditions
: under AHC&HG stress vs AHC&CHH stress

III. Mechanism of degradation under repeated stress

To investigate the degradation phenomenon under repeated stress, difference(Δ Vt') between Δ Vt [repeated stress] and Δ Vt[only AHC stress] after the stress of 3000 seconds was evaluated as a function of Vd under AHC stress conditions as shown in Fig.3. HG stress were applied after each AHC stress of 1000 seconds. These results reveal that the enhanced degradation under repeated stress is considerably affected by the amount of new trap centers generated by AHC injection.

To clarify the mechanism of the degradation, difference(Δ Vt') between Δ Vt [repeated stress] and Δ Vt[only AHC stress] was evaluated using pMOSFETs with different oxide thickness(10nm and 16nm) as shown in Fig.4. Very large changes of Δ Vt' are observed for the devices with gate oxide of 10nm but only small changes of Δ Vt' are observed for that with gate oxide of 16nm. Further, Δ Vt under HG stress after the AHC injection was evaluated as shown in Fig.5. Large changes of Δ Vt at gate oxide of 10nm is observed but slight change of Δ Vt at gate oxide of 16nm is observed. We have confirmed that without pre-AHC injection slight change of Δ Vt at gate oxide of 10nm is observed even under HG stress. These results reveal that for the device with thin gate oxide(~10nm), a large number of electron traps occur and simultaneously a large number of new hole trap centers are generated by AHC injection. Subsequently, trapped electrons are more and less neutralized due to holes which are trapped into the new hole trap centers and at the same time a large number of new electron trap centers are generated. Conseqently, the degradation is enhanced due to electron traps which are caused by each AHC injection.

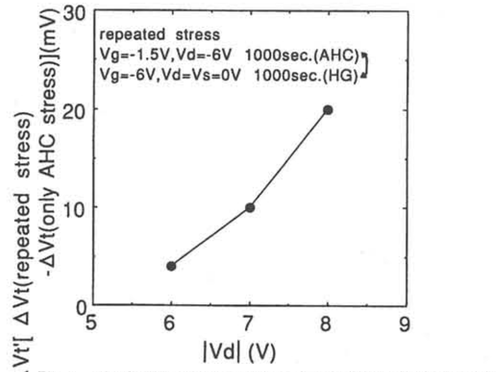

Fig.3. Δ Vt'[Δ Vt(repeated stress)- Δ Vt(only AHC stress)] dependent of Vd under AHC stress

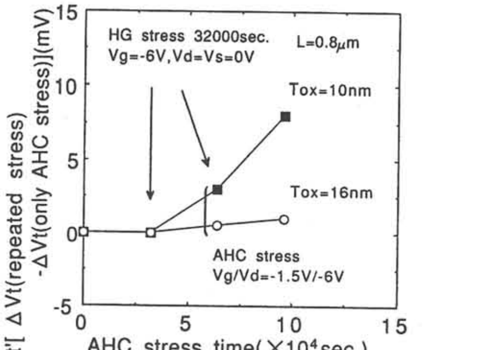

Fig.4. Δ Vt'[Δ Vt(repeated stress)- Δ Vt(only AHC stress)] dependent of gate oxide thickness under repeated stress
: at gate oxide of 10nm vs at gate oxide of 16nm

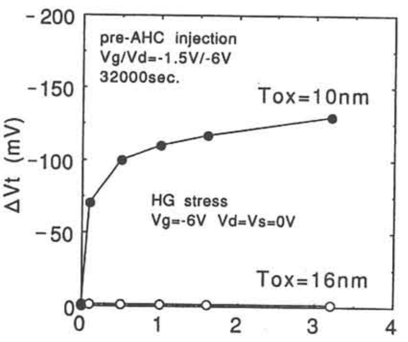

Fig.5. Δ Vt under HG stress after AHC injection
: at gate oxide of 10nm vs at gate oxide of 16nm

To clarify a factor which causes the enhanced degradation, dependence of difference(Vgd) between the gate voltage and the drain voltage under HG stress was evaluated as shown in Fig.6. For example, obvious difference of Δ Vt between repeated stress at Vgd=-6V and that at Vgd=-4V is observed after the stress of 10^5 seconds. The degradation under AHC stress after HG stress at Vgd=-6V is more enhanced compared to that at Vgd=-4V. These results reveal that the enhanced degradation under the repeated stress is occurred since avalanche hot electrons are trapped into the new electron trap centers which are generated by hole injection with high energy at high Vgd even under short HG stress time as shown in Fig.5. Consequently, avalanche hot electrons are considerably injected into the gate oxide under subsequent each AHC stress which keeps high lateral electric field. On the other hand holes which are generated by CHH stress are trapped into the gate oxide,too. However, these holes do not generate much new electron trap centers.

Finally, LDD dose dependence of difference(Δ Vt') between Δ Vt [repeated stress] and Δ Vt[only AHC stress] was evaluated as shown in Fig.7. It is noted that Δ Vt' increases with LDD dose. Since effective electric field between gate and drain increases with LDD dose, the degradation is enhanced. A model of degradation under repeated stress is shown in Fig.8. It is indicated that holes under HG stress are trapped into the new hole trap centers which are generated by AHC stress in the gate oxide and at the same time these holes generate new electron trap centers in the gate oxide above the drain.

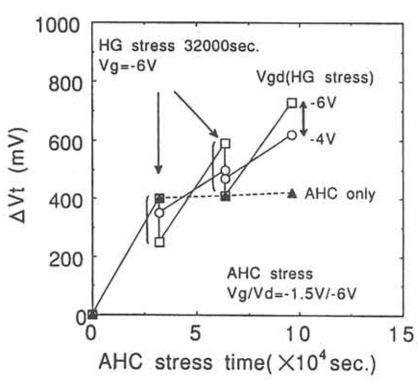

Fig.6. ΔVt dependent of Vgd(Vgs) under HG stress

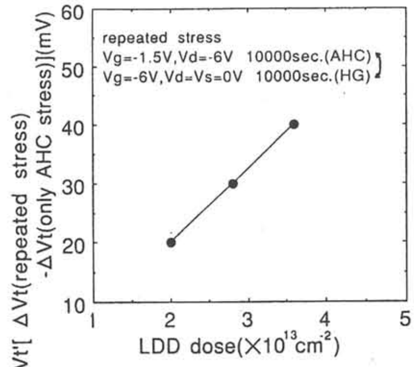

Fig.7. ΔVt'[ΔVt(repeated stress)-ΔVt(only AHC stress)] dependent of LDD dose under repeated stress

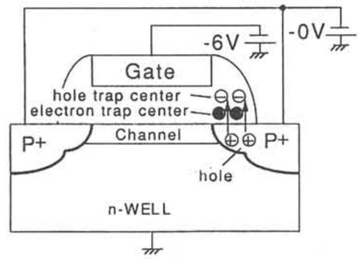

Fig.8. Model of hole injection into the new trap centers in the gate oxide above the drain under high gate and low drain voltage stress

IV. Conclusions

A new enhanced degradation phenomenon of LDD pMOSFETs has been clarified under repetition of HG stress and AHC stress where drain current is not flowing. This enhanced degradation is especially observed in pMOSFETs with thin gate oxide(~10nm). A large number of new trap centers are generated by avalanche hot electron injection into the gate oxide, and then holes with high energy are trapped into the new trap centers in the gate oxide above the drain even during short high gate and low drain voltage stress time and at the same time these holes generate new electron trap centers in the gate oxide.

We have demonstrated the mechanism of device degradation on CMOS inverter operations in LSI circuits using repetition of AHC stress and HG stress methods , which can not be achieved by AHC stress tests alone, thus implying the practical significance of both AHC and HG stress.

V. Acknowledgement

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References

[1] T.Tsuchiya et al., IEEE Transaction on Electron Devices.vol.ED-34, NO.2, p386 , 1987.